

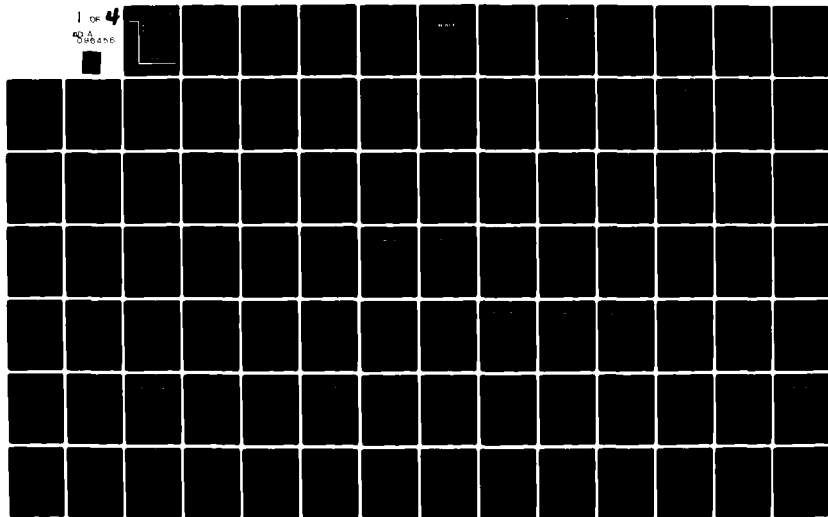
AD-A096 456

TELEDYNE BROWN ENGINEERING HUNTSVILLE ALA SYSTEMS DIV F/G 9/2
SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
FEB 81 S J CLYMER F33615-78-C-0013

UNCLASSIFIED

AFHRL-TR-80-42-PT-2 NL

1 OF 4
80A
DUPLICATE



AFHRL-TR-80-42 (Part II)

AIR FORCE



AD A 096456

HUMAN RESOURCES

LEVEL II

12

SOFTWARE PARTITIONING SCHEMES FOR ADVANCED
SIMULATION COMPUTER SYSTEMS

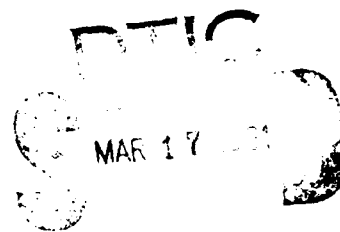
By

S. J. Clymer
Systems Division
Teledyne Brown Engineering
300 Sparkman Drive
Huntsville, Alabama 35807

OPERATIONS TRAINING DIVISION
Williams Air Force Base, Arizona 85224

February 1981

Final Report



Approved for public release; distribution unlimited.

LABORATORY

AIR FORCE SYSTEMS COMMAND
BROOKS AIR FORCE BASE, TEXAS 78235

81 3 17 033

USE FILE

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This final report was submitted by Systems Division, Teledyne Brown Engineering, 300 Sparkman Drive, Huntsville, Alabama 35807, under Contract F33615-78-C-40013, Project 6114, with the Operations Training Division, Air Force Human Resources Laboratory (AFSC), Williams Air Force Base, Arizona 85224. Pat Price was the Contract Monitor for the Laboratory.

This report has been reviewed by the Office of Public Affairs (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

MARTY R. ROCKWAY, Technical Director
Operations Training Division

RONALD W. TERRY, Colonel, USAF
Commander

Unclassified

(19) TR 80-42 P7-6

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFHRI-TR-80-42 (Part II)	2. GOVT ACCESSION NO. AD-A096433	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER SYSTEMS. Part II.	5. TYPE OF REPORT & PERIOD COVERED Final report	
7. AUTHOR(s) S.J. Clymer	6. PERFORMING ORG. REPORT NUMBER	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Systems Division, Teledyne Brown Engineering 300 Sparkman Drive Huntsville, Alabama 35807	8. CONTRACT OR GRANT NUMBER(s) F33615-78-4-4013	
11. CONTROLLING OFFICE NAME AND ADDRESS HQ Air Force Human Resources Laboratory (AFSC) Brooks Air Force Base, Texas 78235	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62205F 61142301	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Operations Training Division Air Force Human Resources Laboratory Williams Air Force Base, Arizona 85234	12. REPORT DATE Feb 1981	
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	17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)	
18. SUPPLEMENTARY NOTES This report consists of two parts. Part I includes pages 1 through 152. Part II contains pages 153 through 460.		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) multiple processors software partitioning real-time computational design evaluation flight simulation data base management software design computer systems		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The overall objective of this study was to design software partitioning techniques that can be used by the Air Force to partition a large flight simulator program for optimal execution on alternative configurations. The results were a mathematical model which defines characteristics for an optimal partition and a manually demonstrated partitioning algorithm design which implements heuristic controls based on the mathematical model statement.		

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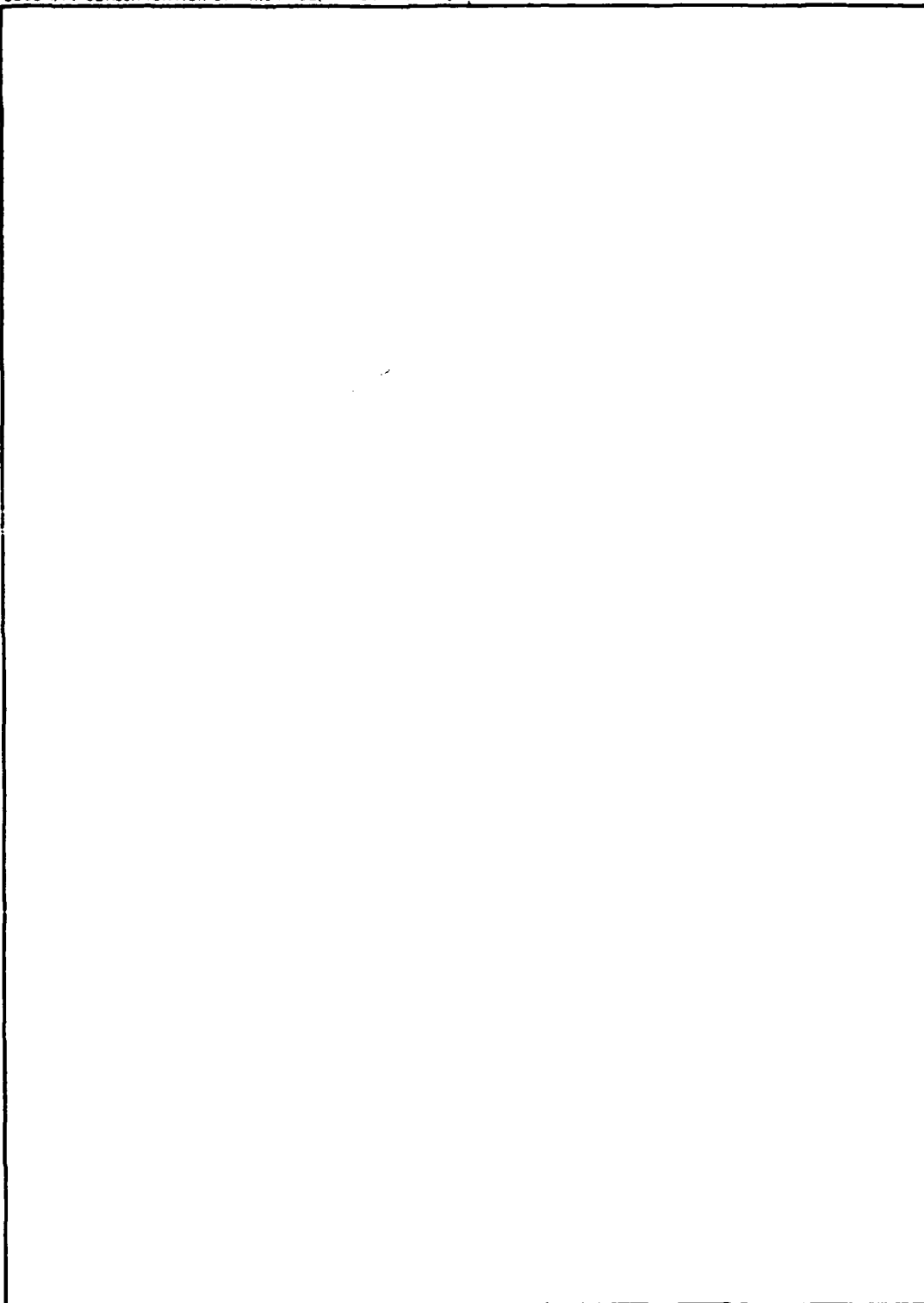
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APPENDIX C. FEASIBILITY DEMONSTRATION

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C.1 VIEWGRAPHS

FINAL BRIEFING

Software Partitioning Schemes
for
Advanced Simulation Computer Systems

CONTRACT F 33615-78-C-0013

CDRL ITEM 6

Prepared by
TELEDYNE BROWN ENGINEERING

AGENDA

- **PROJECT SUMMARY**
 - **SCHEDULE AND APPROACH OBJECTIVES**
 - **DESIGN GOALS AND ALTERNATIVES**
 - **RESULTS**

- **PARTITIONING ALGORITHM DESIGN**
 - **ORGANIZATION OF DESIGN MATERIALS**
 - **FEASIBILITY DEMONSTRATION**
 - **DETAILED DESIGN REVIEW**

PROJECT SUMMARY

⇒ ● SCHEDULE AND APPROACH OBJECTIVES

- PROJECT OBJECTIVES**
- MILESTONE SCHEDULE**
- LITERATURE SEARCH**
- FLIGHT TRAINER ANALYSIS**
- DESIGN**

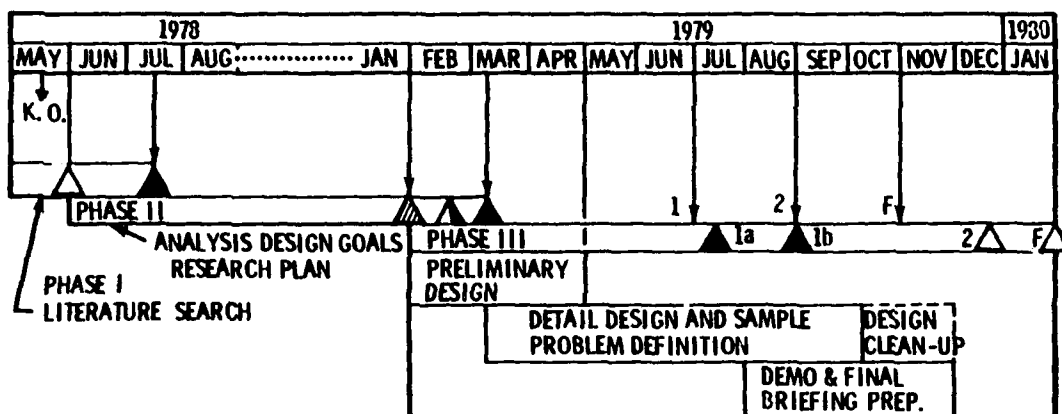
● DESIGN GOALS AND ALTERNATIVES

● RESULTS AND RECOMMENDATIONS

PROJECT OBJECTIVES

- **RESEARCH FLIGHT TRAINING SIMULATORS**
- **ANALYZE FLIGHT TRAINING SIMULATORS**
- **DESIGN A SOFTWARE PARTITIONING
ALGORITHM TAILORED TO FLIGHT
TRAINING SIMULATOR PROBLEMS**
- **DEMONSTRATE THE ALGORITHM'S CAPABILITIES**
- **RECOMMEND UTILIZATION/AUTOMATION**

MILESTONE SCHEDULE



LITERATURE SEARCH

- **GOVERNMENT AGENCIES**
- **MILITARY CONTRACTORS**
- **COMMERCIAL AIRLINES**
- **TECHNICAL PUBLICATIONS**
- **DOD ABSTRACTS**
- **NASA ABSTRACTS**

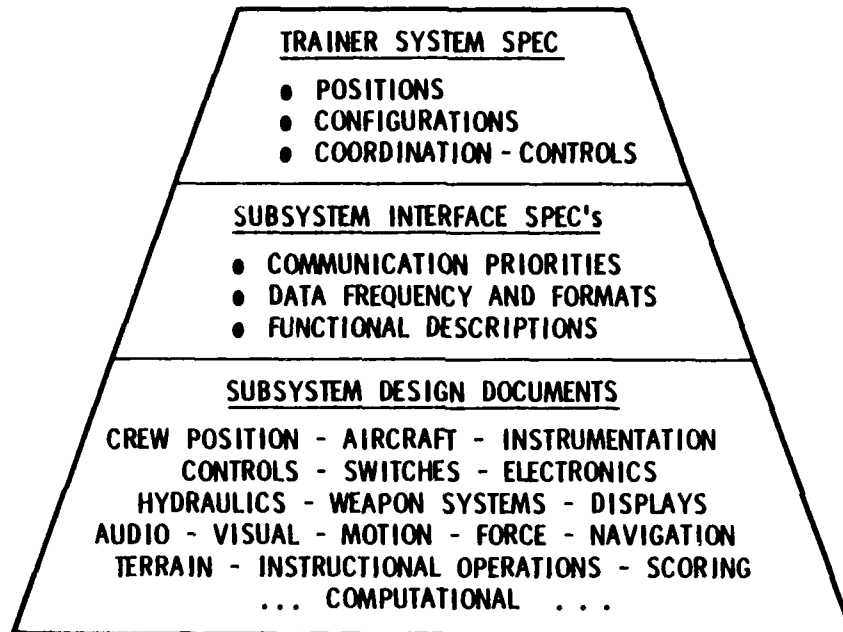
LITERATURE SEARCH

KEY INFORMATION SOURCES

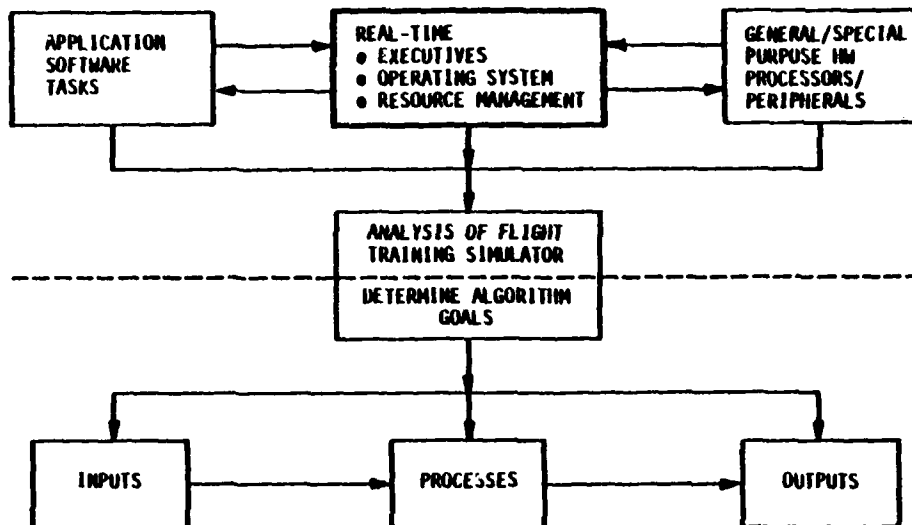
- ASUPT '74 & '76 DOCUMENTS
- ASPT VISUAL SUBSYSTEM EXPANDED PDR
- DEVICE 2E6 TRAINING ENGINEERING
DESIGN REPORT
- SPECIFICATION FOR AIR COMBAT
MANEUVERING SIMULATOR DEVICE 2E6

LITERATURE SEARCH

HIERARCHY OF FLIGHT TRAINER DOCUMENTS



FLIGHT TRAINER ANALYSIS



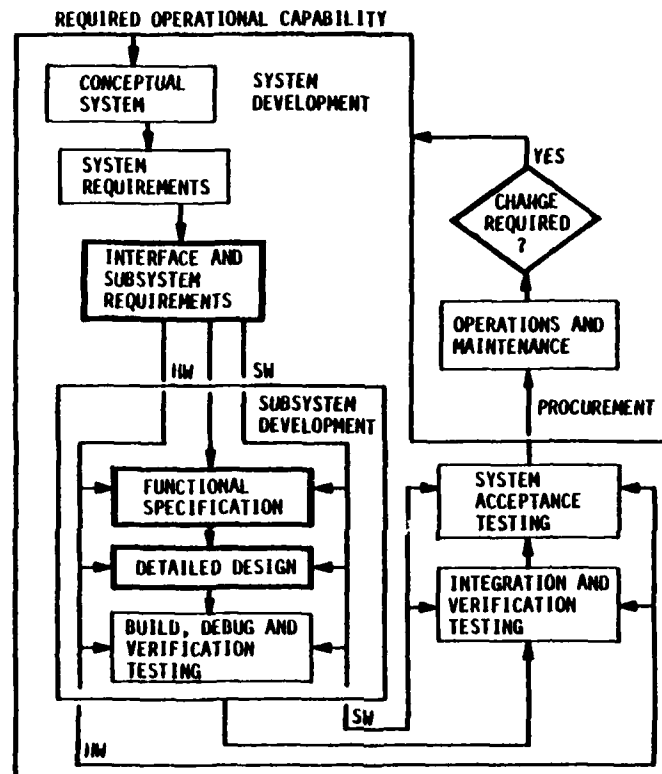
DESIGN CONSIDERATIONS

OPERATIONAL ENVIRONMENT QUESTIONS

- **AT WHAT POINT(S) IN THE SYSTEM DEVELOPMENT CYCLE IS THE ALGORITHM TO BE USED?**
- **WHAT TIME FRAME AND COMPUTER RESOURCES ARE ANTICIPATED FOR CANDIDATE EVALUATIONS?**
- **WHAT FORMAT AND TO WHAT EXTENT WILL THE SYSTEM REQUIREMENTS BE DOCUMENTED?**
- **WHAT FORMAT AND TO WHAT EXTENT WILL THE ALTERNATE CANDIDATE DESIGN CONFIGURATIONS BE DOCUMENTED?**

DESIGN CONSIDERATIONS

ALGORITHM RELATIONS WITH THE SYSTEM LIFE CYCLE



PROJECT SUMMARY

- **SCHEDULE AND APPROACH OBJECTIVES**

- ⇒ • **DESIGN GOALS AND CONSIDERATIONS**

- **GOALS**

- **ALTERNATIVES**

- **GOAL PROGRAM ENGLISH STATEMENT**

- **HEURISTIC GOAL PROGRAM DECISION MODELS**

- **RESULTS AND RECOMMENDATIONS**

DESIGN GOALS

- **PARTITION TASKS TO A USER SPECIFIED MULTIPROCESSOR
HARDWARE CONFIGURATION**
- **IDENTIFY INTERDEPENDENCIES AMONG THE TASKS**
- **PRECLUDE SYSTEM DEADLOCKS**
- **BALANCE THE PROCESSING LOAD**
- **CROSS REFERENCE TASK(S) ASSIGNED TO PROCESSORS**
- **LIST CRITICAL CONSTRAINTS WHEN A VALID PARTITION
IS NOT OBTAINABLE**
- **PROVIDE A DEVELOPMENT COST ESTIMATE**

DESIGN ALTERNATIVES

LINEAR PROGRAMMING
VERSUS
GOAL PROGRAMMING

MIXED INTEGER
VERSUS
CONTINUOUS
SOLUTIONS

OPTIMIZER
VERSUS
HEURISTIC

INITIAL ALLOCATION
USER SUPPLIED
VERSUS
AUTOMATIC GENERATION

GOAL PROGRAM ENGLISH STATEMENT

- **COMPETING OBJECTIVES :**
 - **BALANCE THE PROCESSING LOAD AMONG THE PROCESSORS**
 - **BALANCE THE MEMORY STORAGE UTILIZATION**
 - **MINIMIZE DEVELOPMENT COSTS**
- **SUBJECT TO :**
 - **REAL-TIME TASK RESOURCE REQUIREMENTS**
 - **PERFORMANCE SIMULATION FEEDBACK**

GOAL PROGRAM SIZING

CASE	CONTROL PARAMETERS						RESULTANT MATRIX		
	T TASKS	P PROC	B BLOCKS	M MEM	I IMPUTE	O OUTPUT	VARIABLES	ROWS	COLUMNS
1	30	2	61	3	3	2	1330	1747	4824
2	30	3	61	4	3	2	2383	3009	8401
3	30	3	120	4	3	3	3038	3608	10224
4	30	3	120	6	3	3	4358	4688	13734
5	60	4	140	6	3	3	10351	12271	34893
PROB 1	5	2	12	3	3	3	264	348	960
PROB 2	7	4	21	6	3	3	1250	1642	4534
<p>VARIABLES = $B + P + M + 1 + MB + 3TP + TPM (I + O)$</p> <p>ROWS = $B + P + M + 1 + 2T + 2TP (1 + I + O) + TMP (I + O)$</p> <p>COLUMNS = $VARIABLES + 2 (ROWS)$</p>									

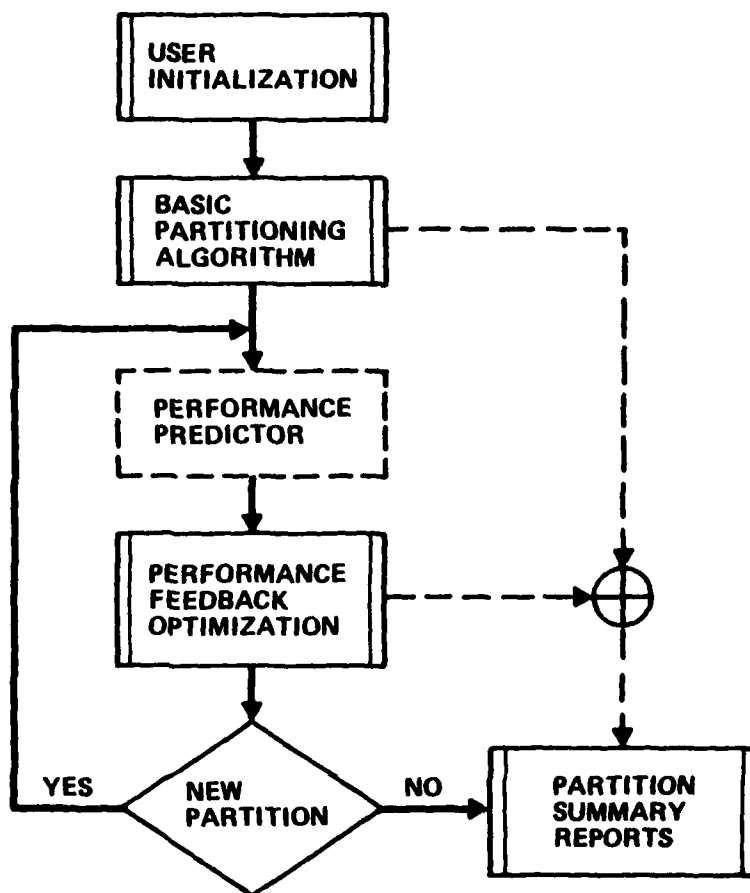
HEURISTIC GOAL PROGRAM DECISION MODELS

- GENERALLY REQUIRE AN INITIAL FEASIBLE ALLOCATION
- TAILORED TO SPECIFIC APPLICATION MODEL RELATIONSHIPS
- SEEK AN "IMPROVED" ALLOCATION SOLUTION WHICH MAY NOT NECESSARILY BE THE GLOBAL OPTIMUM
- PREEMPTIVE PRIORITY TECHNIQUES CAN BE EMPLOYED FOR MULTIPLE OBJECTIVES
- FOR LARGE PROBLEMS (MORE THAN SEVERAL HUNDRED VARIABLES OR CONSTRAINTS) HEURISTICS TEND TO BE COMPUTATIONALLY MORE EFFICIENT THAN A GENERALIZED OPTIMIZER IN PROVIDING ANSWERS TO USERS
- ONLY IMMEDIATE DECISION PARAMETERS ARE REQUIRED "IN MEMORY"

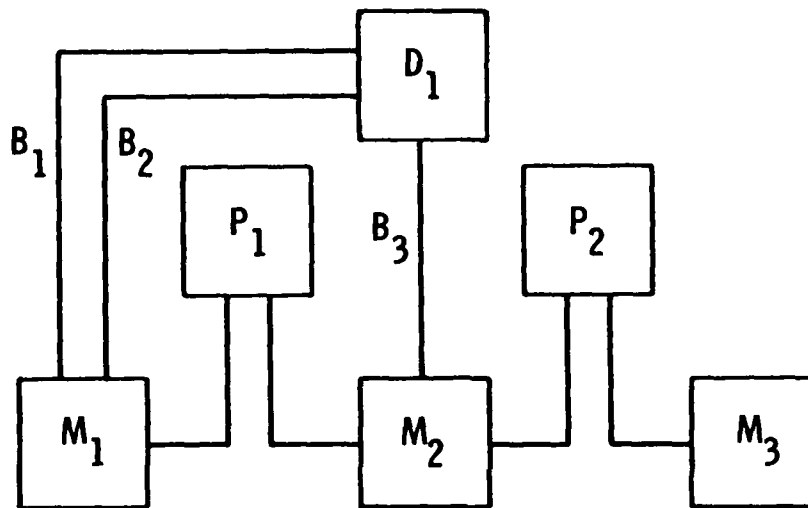
PROJECT SUMMARY

- SCHEDULE AND APPROACH OBJECTIVES
- DESIGN GOALS AND ALTERNATIVES
- ⇒ • RESULTS AND RECOMMENDATIONS
 - ALGORITHM COMPUTATIONAL STEPS
 - SIMPLIFIED PROBLEM
 - SOURCE OF INPUTS
 - RECOMMENDED AUTOMATED IMPLEMENTATION TASKS
 - RECOMMENDED IMPLEMENTATION TIMELINE
 - FURTHER STUDY REQUIREMENTS

ALGORITHM COMPUTATIONAL STEPS



SIMPLIFIED PROBLEM CONFIGURATION



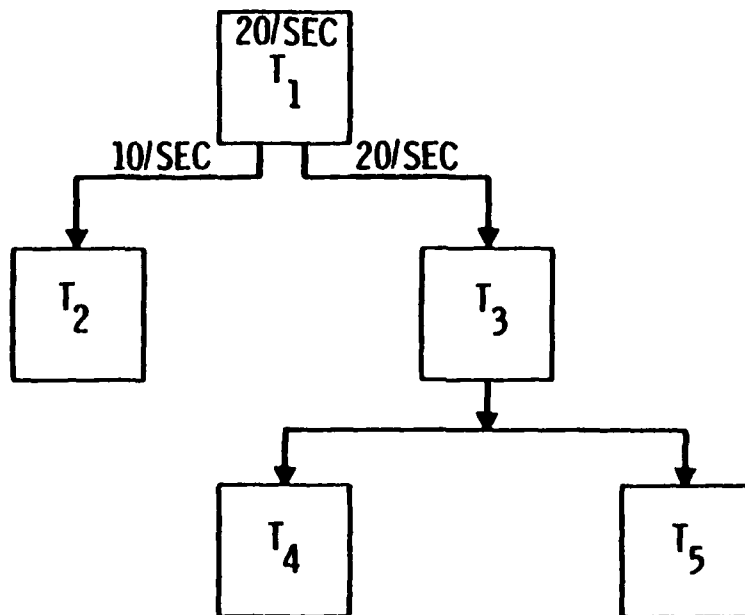
1 DEVICE

3 MEMORIES

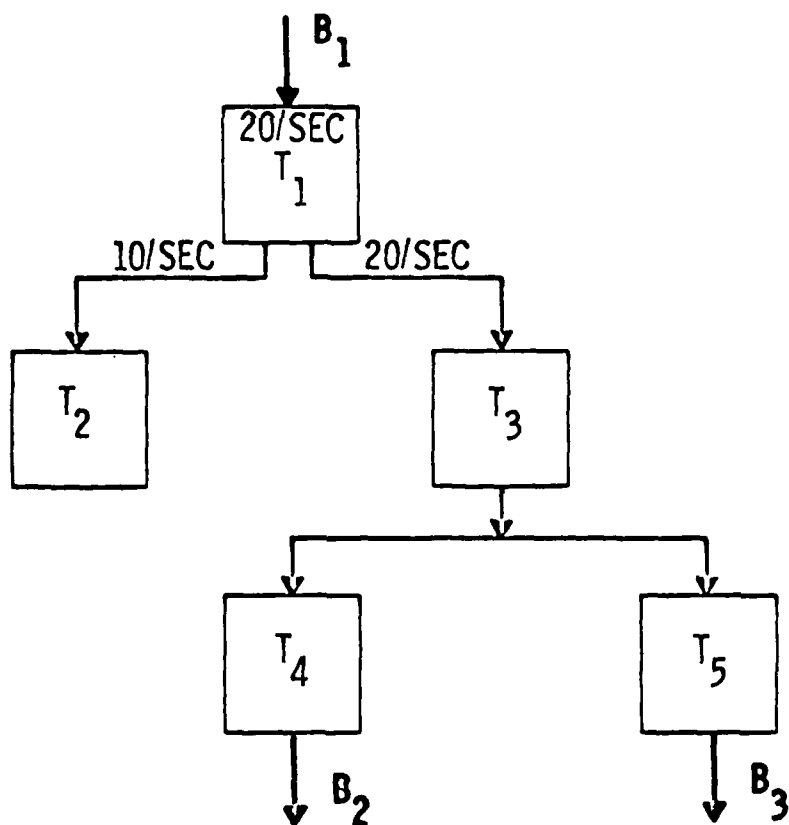
2 PROCESSORS

3 BUFFERS

SIMPLIFIED PROBLEM APPLICATION

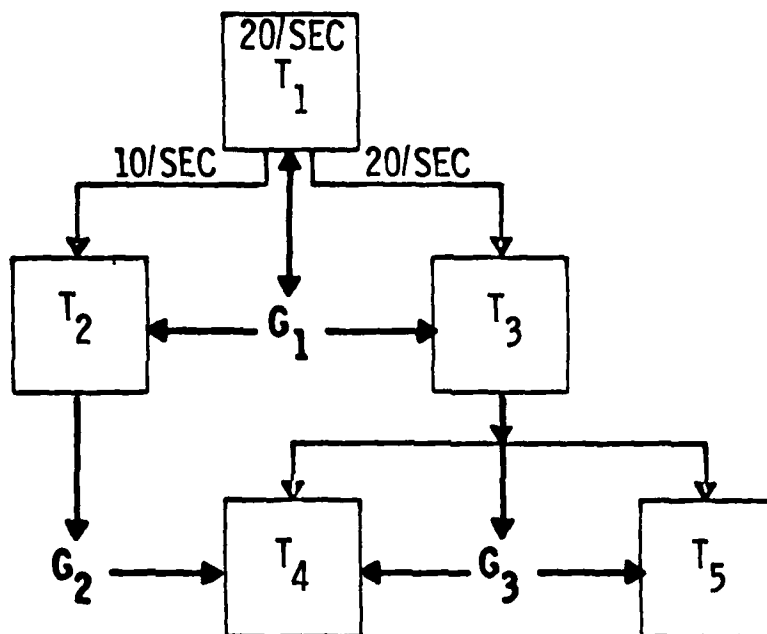


SIMPLIFIED PROBLEM APPLICATION



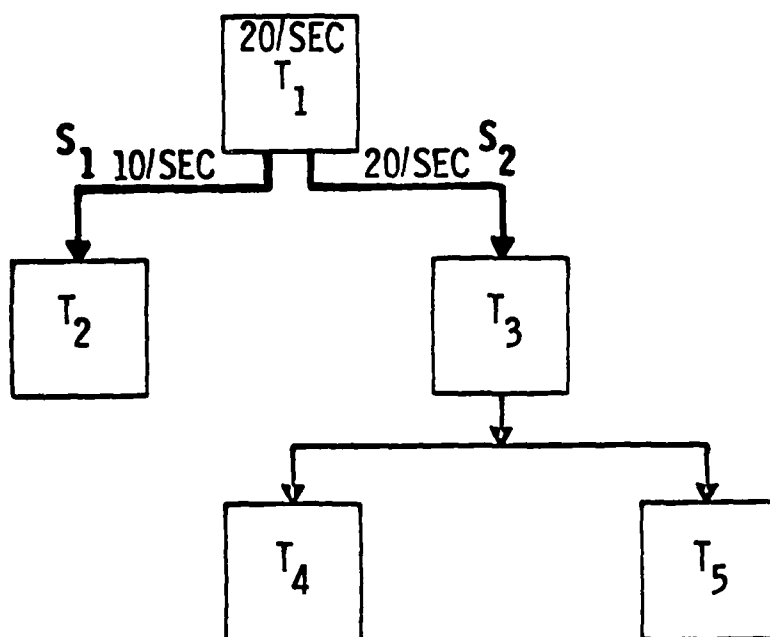
EXTERNAL I/O

SIMPLIFIED PROBLEM APPLICATION



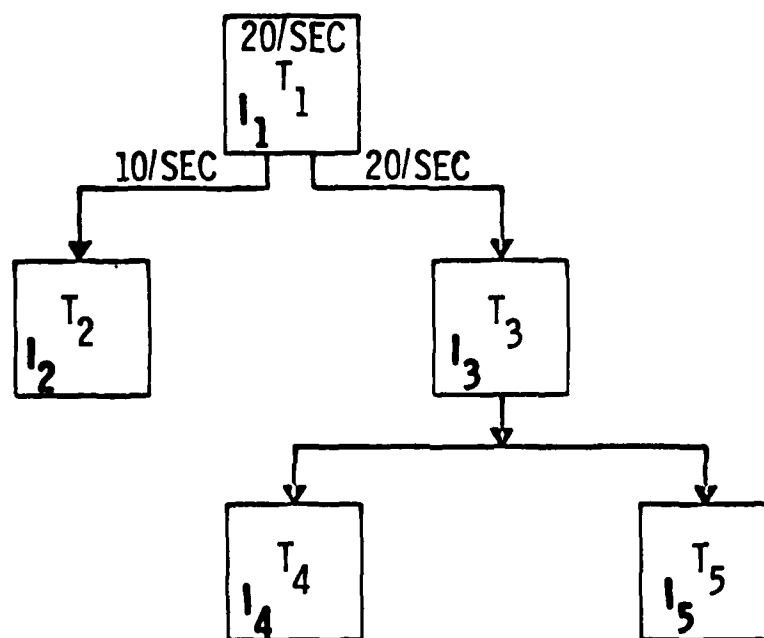
GLOBAL I/O

SIMPLIFIED PROBLEM APPLICATION



SEQUENTIAL I/O

SIMPLIFIED PROBLEM APPLICATION



INSTRUCTION BLOCKS

SIMPLIFIED PROBLEM OUTPUT FORMAT 101

PRIORITY GOAL SUMMARY

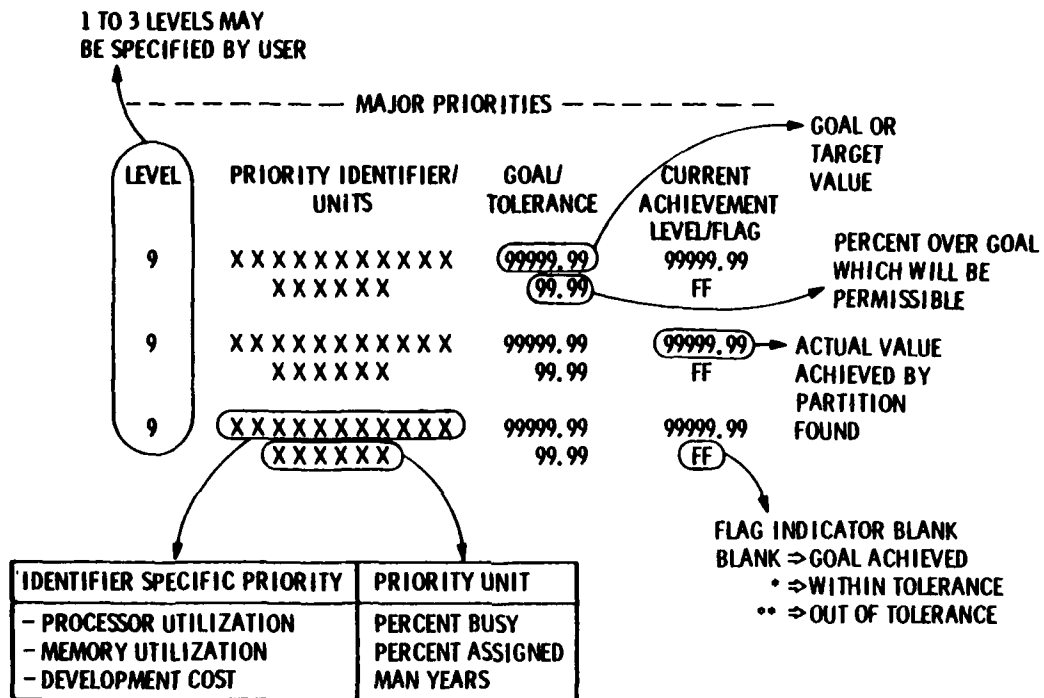
----- MAJOR PRIORITIES -----				----- PRIORITY COMPONENTS -----			
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE	CURRENT ACHIEVEMENT LEVEL / FLAG	COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL / FLAG
1	PROCESSOR UTILIZATION % BUSY	60.00 5.00%	60.00	P1	60	5.00	60
				P2	60	5.00	60
2	DEVELOPMENT COST MANYEARS	5.00 10.00%	5.60 ..	T1	.5	10.00	.5
				T2	1.0	10.00	1.0
				T3	1.0	5.00	1.5 ..
				T4	.5	1.00	.5
				T5	2.0	10.00	2.0
3	MEMORY UTILIZATION % ASSIGNED	60.00 5.00%	53.00	M1	60	5.00	66.00 ..
				M2	30	2.00	32.00
				M3	60	5.00	59.00

PRIORITY GOAL SUMMARY

----- MAJOR PRIORITIES -----				----- PRIORITY COMPONENTS -----			
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE	CURRENT ACHIEVEMENT LEVEL/FLAG	COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL FLAG
0	XXXXXXXXXXXXXXXX XXXXXXXX	00000.00 00.00	00000.00 FF	XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF
0	XXXXXXXXXXXXXXXX XXXXXXXX	00000.00 00.00	00000.00 FF	XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF
0	XXXXXXXXXXXXXXXX XXXXXXXX	00000.00 00.00	00000.00 FF	XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF
				XXXXXXXX0000	00000.00	00.000	00000.00 FF

----- USER SUPPLIED PRIOR TO PARTITIONING
 ----- USER IMPLIED PRIOR TO PARTITIONING
 ----- USER MAY SUPPLY OR IMPLY PRIOR TO PARTITIONING
 ----- RESULTANT PARTITION MEASUREMENT

MAJOR PRIORITY PARAMETERS



PRIORITY COMPONENT PARAMETERS

----- PRIORITY COMPONENTS -----				
COMPONENT	GOAL	TOLERANCE PERCENT	CURRENT ACHIEVEMENT LEVEL	FLAG
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF
XXXXXX9999	99999.99	99.999	99999.99	FF

PROCESSOR ID
MEMORY ID
TASK ID

GOAL OR TARGET
DEVELOPMENT FOR
GIVEN COMPONENT

MAXIMUM ACCEPTABLE
DEVIATION ABOVE
TARGET

LEVEL ACTUALLY
ACHIEVED BY
PARTITIONING
ALGORITHMS

ACHIEVEMENT FLAG
 * => ABOVE GOAL BUT
 WITHIN TOLERANCE
 ** => OUT OF TOLERANCE

SIMPLIFIED PROBLEM OUTPUT FORMAT 102

TASK	PROCESSOR	EXECUTIONS	TOTAL TIME	FLAG	TASK ALLOCATION			
					TASK I/O			
					BLOCK	MEMORY	INPUT	OUTPUT
T1	P1	20/20	.20		I1	M1	✓	✓
					B1	M1	✓	
					G1	M2	✓	✓
					S1	M1		✓
					S2	M2		✓
T2	P1	10/10	.20		I2	M1	✓	
					G1	M2	✓	
					G2	M2		✓
					S1	M1	✓	
T3	P2	20/20	.20		I3	M3	✓	
					G1	M2	✓	
					G3	M2		✓
						M3		✓
					S2	M2	✓	
T4	P1	20/20	.20		I4	M1	✓	
					B2	M1		✓
					G2	M2	✓	
					G3	M2	✓	
T5	P2	20/20	.40		I5	M3	✓	✓
					B3	M2		✓
					G3	M3	✓	

TASK ALLOCATION SUMMARY

TASK ALLOCATION									
TASK	PROCESSOR	EXECUTIONS		TOTAL		TASK I/O			
				TIME	FLAG	BLOCK	MEMORY	INPUT	OUTPUT
XXXXXX	XXXXXXXX9999	999/	999	9.99999	FF	XXXXXX	XXXXXXXX9999	9.999999	9.999999
						XXXXXX	XXXXXXXX9999	9.999999	9.999999
						XXXXXX	XXXXXXXX9999	9.999999	9.999999
	XXXXXXXX9999	999/	999	9.99999	FF	XXXXXX	XXXXXXXX9999	9.999999	9.999999
						XXXXXX	XXXXXXXX9999	9.999999	9.999999
						XXXXXX	XXXXXXXX9999	9.999999	9.999999
XXXXXX	XXXXXXXX9999	999/	999	9.99999	FF	XXXXXX	XXXXXXXX9999	9.999999	9.999999
						XXXXXX	XXXXXXXX9999	9.999999	9.999999

— USER SUPPLIED VIA BASELINE SOFTWARE TASK DESCRIPTIONS,
DATA, AND LOAD TO BE PARTITIONED

-- PARTITION ALLOCATION OR RESULTING MEASURE

PROCESSOR ALLOCATION SUMMARY

----- PROCESSOR UTILIZATION -----

PROCESSOR	TASK	EXECUTIONS	COMPUTATIONAL		INPUT/OUTPUT		RESOURCE MGMT		FLAG
			TIME	PERCENT	TIME	PERCENT	TIME	PERCENT	
XXXXXXXX9999	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF
	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF
	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF
	TOTAL	99999	999.9999	999.99	9.9999	99.99	9.9999	99.99	FF
XXXXXXXX9999	XXXXXX	999	9.9999	99.99	9.9999	99.99	9.9999	99.99	FF

—— USER SUPPLIED VIA CANDIDATE CONFIGURATION INPUTS

--- PARTITIONING ALLOCATION OR RESULTING MEASURE

SIMPLIFIED PROBLEM OUTPUT FORMAT 103

DATA BLOCK ALLOCATION

BLOCK	MEMORY	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
B1	M1	1000	3.1	P1		500		
B2	M1	2000	6.2	P1	1000			
B3	M2	4000	12.5	P2	2000			
G1	M2	4000	12.5	P1	✓	✓		
				P2		✓		
G2	M2	1000	3.1	P1	✓	✓		
G3	M2	1000	3.1	P1		✓		
				P2	✓			
	M3	1000	3.1	P2	✓	✓		
S1	M1	256	.8	P1	✓	✓		
S2	M2	256	.8	P1	✓			
				P2		✓		
I1	M1	2000	6.2	P1	✓	✓		
I2	M1	12000	37.8	P1	✓	✓		
I3	M3	8000	25.0	P2	✓	✓		
I4	M1	4000	12.5	P1	✓	✓		
I5	M3	10000	31.2	P2	✓	✓		

DATA BLOCK ALLOCATION SUMMARY

DATA BLOCK ALLOCATION

BLOCK	MEMORY	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
XXXXXX	XXXXXX9999	999999	99.99	XXXXXX9999	999999	999999	99999999	FF
				XXXXXX9999	999999	999999	99999999	FF
				XXXXXX9999	999999	999999	99999999	FF
	XXXXXX9999	999999	99.99	XXXXXX9999	999999	999999	99999999	FF
XXXXXX	XXXXXX9999	999999	99.99	XXXXXX9999	999999	999999	99999999	FF

- USER SUPPLIED VIA SOFTWARE TASK BLOCK DESCRIPTIONS
- PARTITIONING ALLOCATION OR RESULTING MEASURES

MEMORY ALLOCATION SUMMARY

MEMORY ALLOCATION

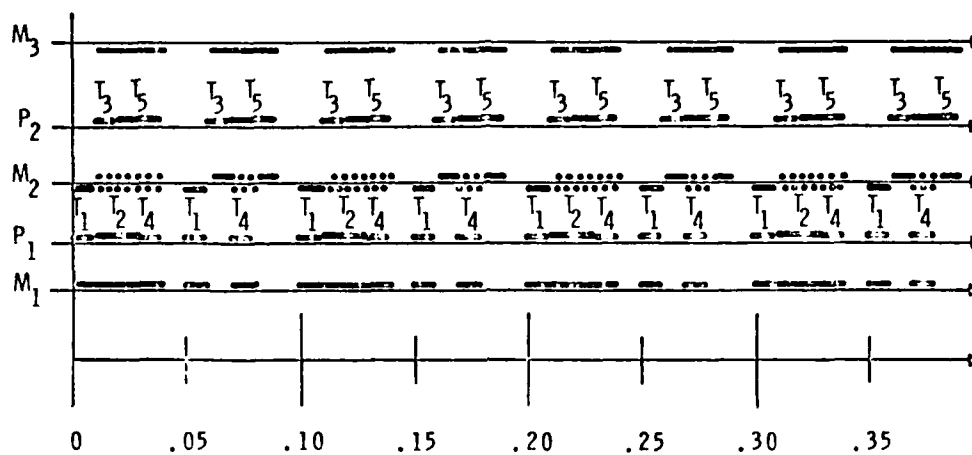
MEMORY	BLOCK	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
XXXXXX9999	XXXXXX	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
	XXXXXX	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
				XXXXXX9999	999999	999999	9999999	FF
	** TOTAL	999999	99.99	XXXXXX9999	999999	999999	9999999	FF
				XXXXXX9999	999999	999999	9999999	FF
				**TOT PROC	9999999	9999999	99999999	FF

—— USER SUPPLIED VIA CANDIDATE CONFIGURATION INPUTS

—— PARTITIONING ALLOCATION OR RESULTING MEASURES

SIMPLIFIED PROBLEM UTILIZATION

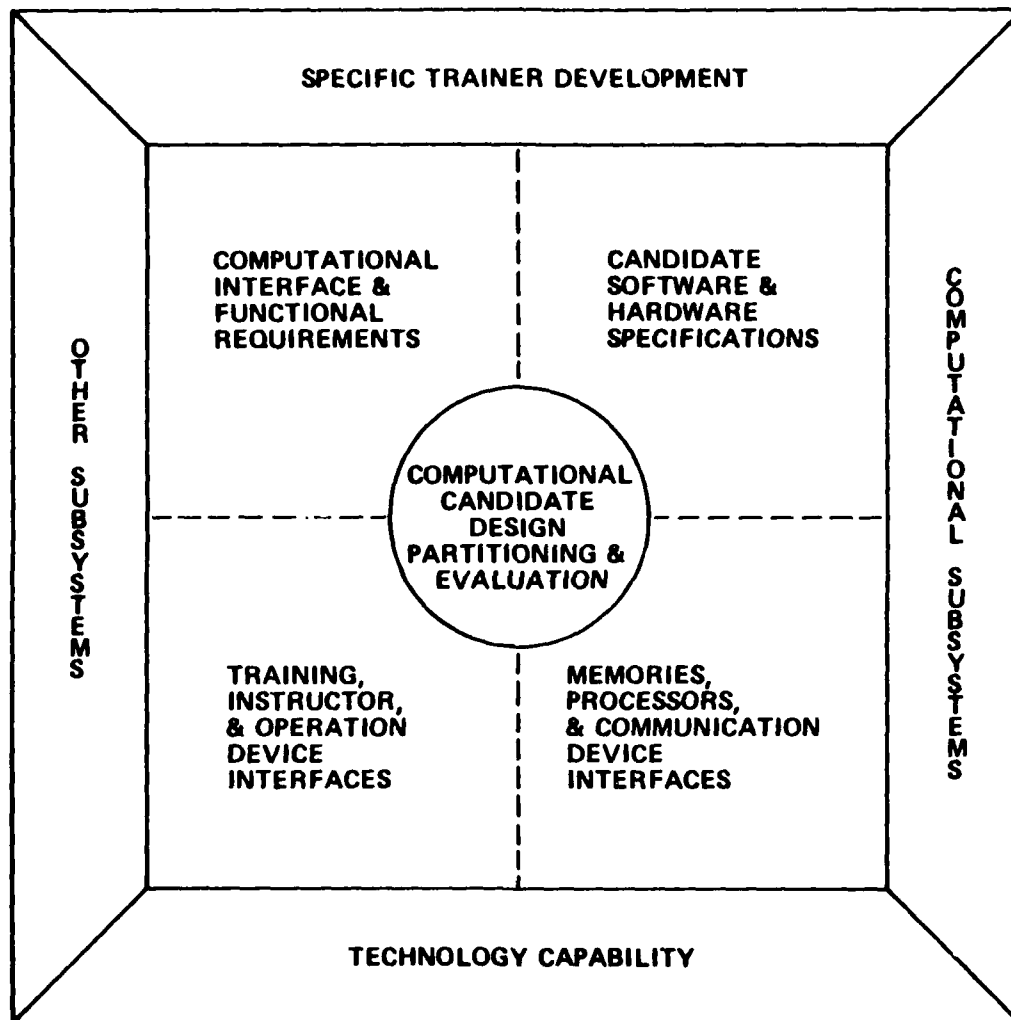
RELATED PERFORMANCE SIMULATION TYPES OF OUTPUT BASED ON STATIC LOAD



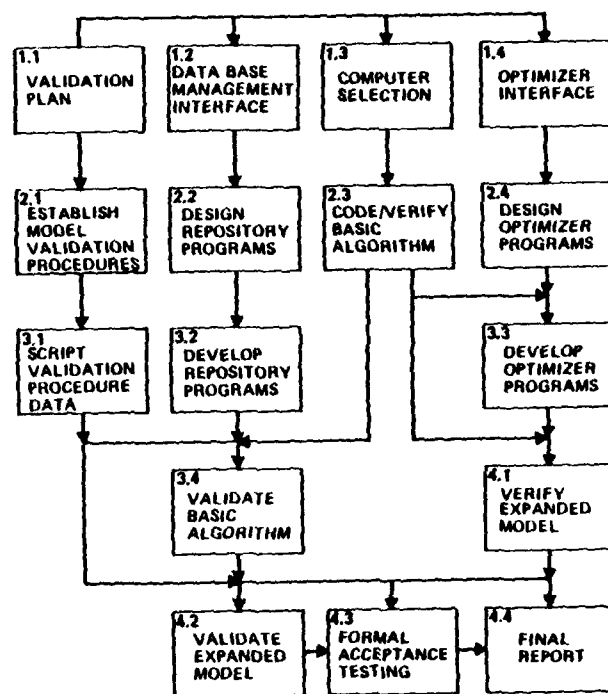
SOURCE OF INPUTS

DOCUMENT(S)	INPUT AREA
COMPUTATIONAL SUBSYSTEM INTERFACE SPECIFICATION	EXTERNAL DEVICE INTERFACES REQUIRED COMPONENTS FUNCTIONAL I/O MAP COMMUNICATION RULES & PRIORITIES BASELINE LOAD(S)
SOFTWARE DESIGN AND DATA BASE SPECIFICATIONS	DATA BLOCK DESCRIPTIONS TASK DESCRIPTIONS TASK THREADS BASELINE LOAD(S) TASKING
HARDWARE CONFIGURATION DESIGN SPECIFICATIONS	PROCESSORS MEMORIES INTERFACES (INTERNAL & EXTERNAL) COMMUNICATION RULES

REPOSITORY SOURCE OF INPUTS



RECOMMENDED AUTOMATED ALGORITHM IMPLEMENTATION TASKS



RECOMMENDED IMPLEMENTATION TIMELINE

PHASE I

TASK DESCRIPTION	MONTH					
	1	2	3	4	5	6
1.1 VALIDATION PLAN			△			◇
1.2 DATA MANAGEMENT PLAN			△			◇
1.3 COMPUTER SELECTION			△			◇
1.4 OPTIMIZER INTERFACE			△			◇

PHASE II

TASK DESCRIPTION	MONTH					
	7	8	9	10	11	12
2.1 VALIDATION PROCEDURES			△			◇
2.2 DESIGN REPOSITORY PROG.			△			◇
2.3 CODE/VERIFY B.A.			△			◇
2.4 DESIGN OPTIMIZER PROG.			△			◇

PHASE III

TASK DESCRIPTION	MONTH								
	13	14	15	16	17	18	19	20	21
3.1 SCRIPT VALIDATION DATA			△						◇
3.2 DEVELOP REPOSITORY PROG.			△						◇
3.3 DEVELOP OPTIMIZER PROG.			△						◇
3.4 VALIDATE BASIC ALGORITHM			△						◇

- △ - INTERIM ON-SITE DEVELOPMENT
PROGRESS REVIEW AND DISCUSSION
- ◇ - DOCUMENTED PRESENTATION TO AF
- - INDEPENDENT ASSESSMENT REPORT

TASK DESCRIPTION	MONTH											
	19	20	21	22	23	24	25	26	27	28	29	30
4.1 VERIFY EXPANDED MODEL			△									
4.2 VALIDATE EXPANDED MODEL			△									
4.3 FORMAL ACCEPTANCE TESTS			△									
4.4 FINAL REPORT			△									

FURTHER STUDY REQUIREMENTS

- **POTENTIAL EMPLOYMENT AND EXPANSION OF
MIXED INTEGER PROGRAM OPTIMIZER**
- **DEVELOPMENT OF MASTER FLIGHT TRAINING
SIMULATOR COMPUTATIONAL SUBSYSTEM
DESIGN REPOSITORY WITH AUTOMATED FILES**

PARTITIONING ALGORITHM DESIGN

- ORGANIZATION OF DESIGN MATERIALS

- ⇒ ● FEASIBILITY DEMONSTRATION

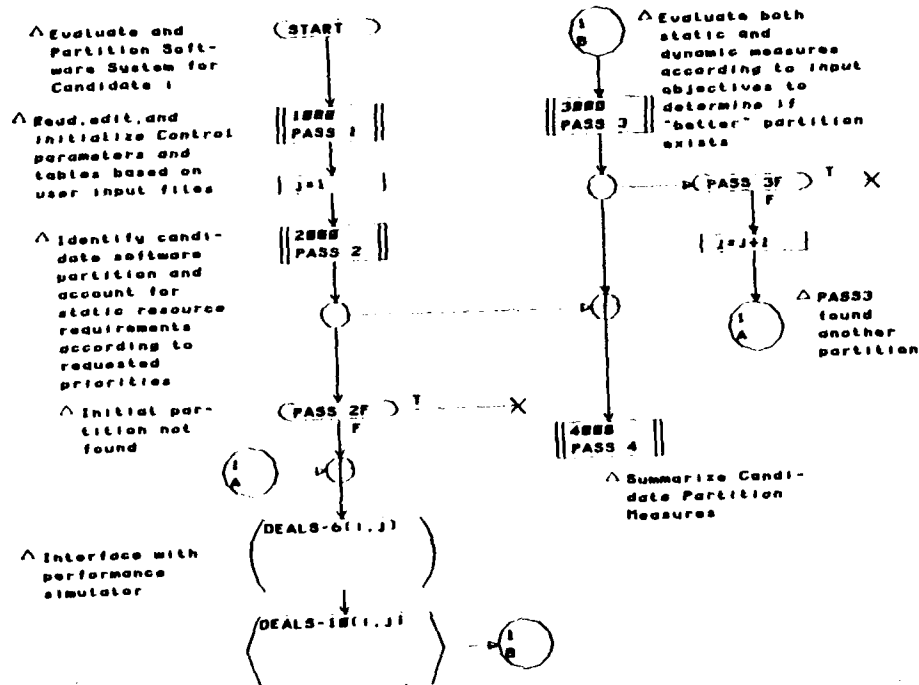
- AREAS ADDRESSED
- USER INPUT PREPARATION
- LOAD BALANCE
- MEMORY BALANCE
- REDUCE DEVELOPMENT COST
- PERFORMANCE BOTTLENECK FEEDBACK
- REPORT GENERATION

- DETAILED DESIGN REVIEW

DEMO AREAS ADDRESSED

- PURPOSE
- PROBLEM
- SOLUTION
- FEASIBILITY ISSUES

DEALS



ISSUE 1 DATE 14-SEP-79 ID DEALS SEC 10RTD-9 PAGE 1

INPUT PROCESSING DEMO

PURPOSE : TO PERMIT AND FACILITATE USER
PARTITIONING PROBLEM DEFINITION

PROBLEM : PARTITIONING REQUIRES CAREFULLY
COORDINATED (YET DIVERSE) SETS OF
DATA BASE PARAMETERS

SOLUTION : MODULAR DATA BASE FILES WHICH ARE
EASILY CROSS-REFERENCED FOR
MINIMIZATION OF REQUIRED AND/OR
REDUNDANT USER INPUTS

INPUT PROCESSING DESIGN

INPUT FILES

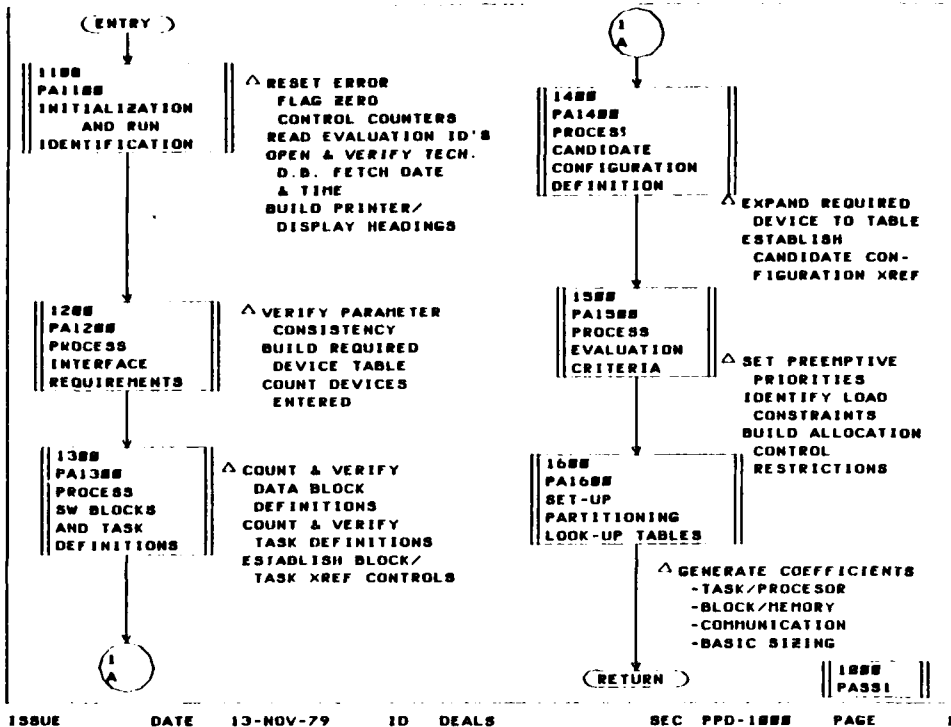
- COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS
- BASELINE SOFTWARE TASK/JOB/LOAD CONFIGURATION
- CANDIDATE HARDWARE CONFIGURATION
- TECHNOLOGY DATA BASE
- EVALUATION CRITERIA AND CONSTRAINTS
- INITIAL ALLOCATION

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

FILE	IDENTIFIER
COMPUTATIONAL INTERFACE REQUIREMENTS	<u>INTERFACE DEFINITION</u>
BASLINE APPLICATION COMPONENTS	<u>SAMPLE APPLICATION</u>
CANDIDATE CONFIGURATION COMPONENTS	<u>SAMPLE CONFIGURATION</u>
BASLINE PARTITIONING LOAD	<u>GLOBAL LOAD EXAMPLE</u>
TECHNOLOGY DATA BASE	<u>HYPOTHETICAL TECH DB</u>

PARTITION LIB

DEALS



ISSUE

DATE

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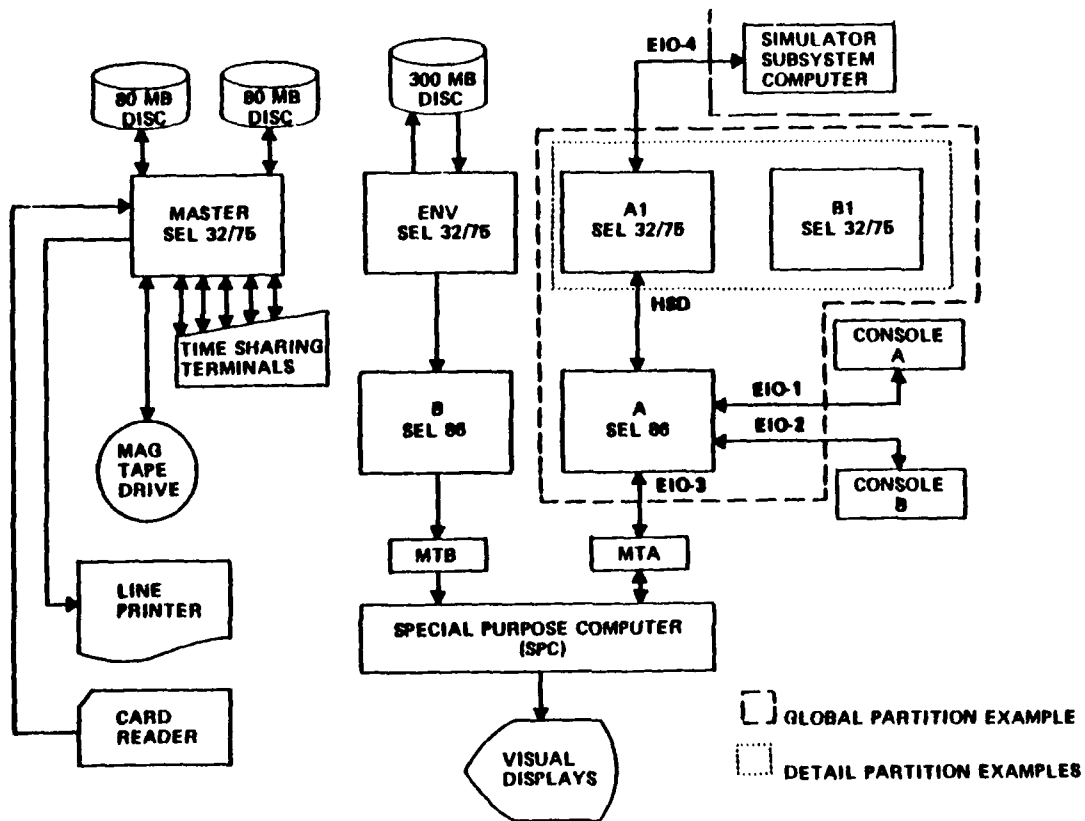
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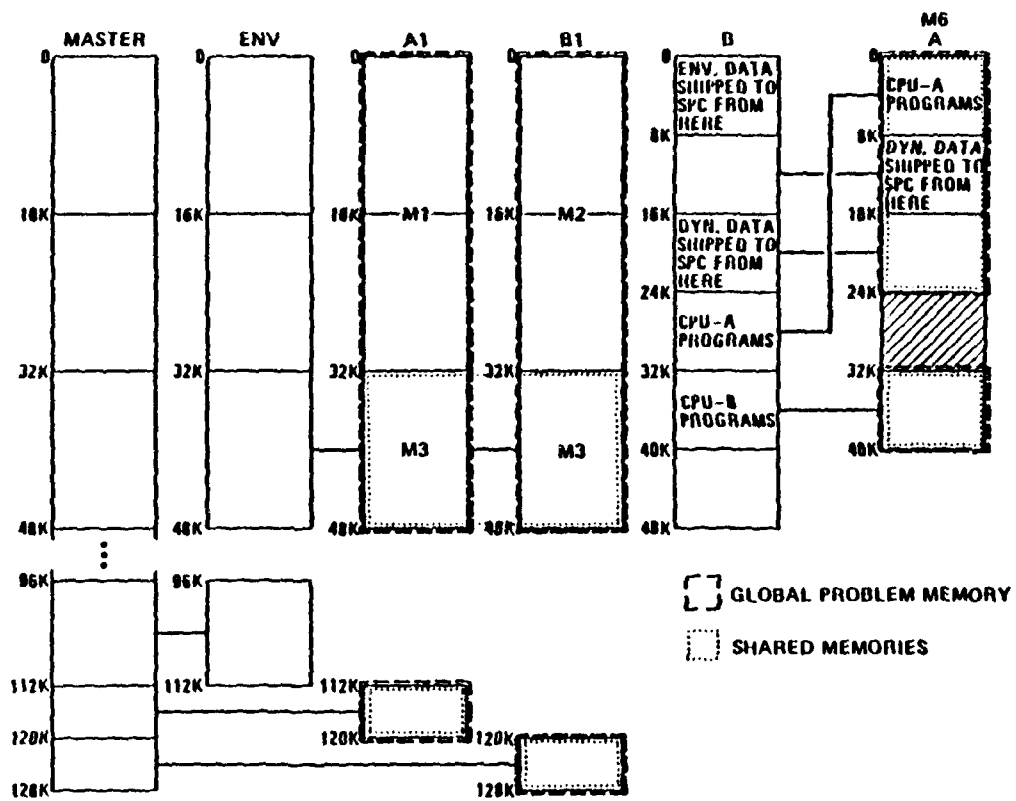
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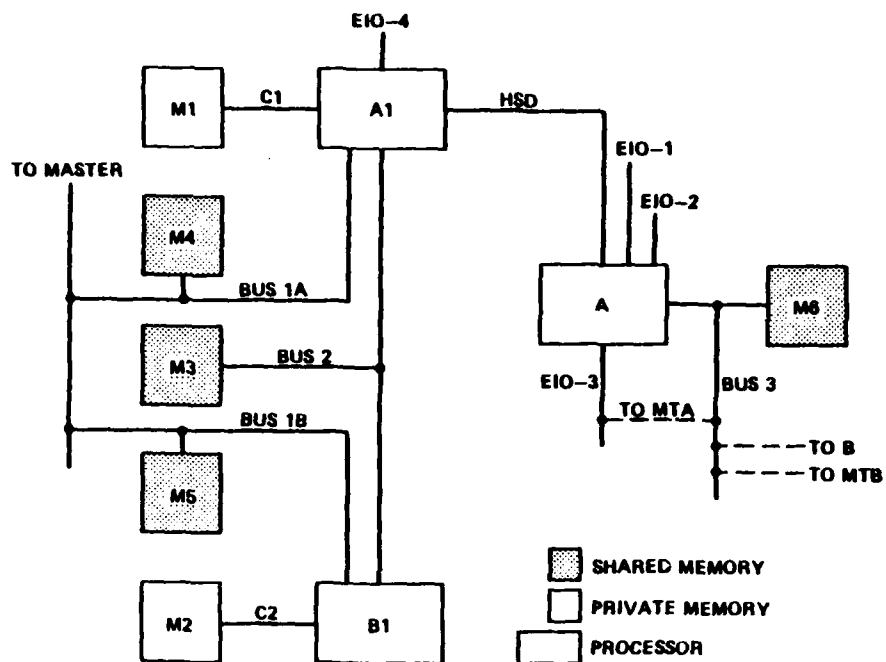
PROCESSOR CONFIGURATION



MEMORY CONFIGURATIONS



SAMPLE CONFIGURATION MEMORY PROCESSOR COMMUNICATIONS



COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS FILE IDENTIFIER INTERFACE DEFINITION

REQUIRED COMPONENTS

COMPONENT		UNIQUE SYSTEM IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
PU	86-PROC	A	8	CUSTOM-VIS	ASSEMBLER	C
			FORTRAN IV	MACRO-ASM		U
PM	SPC	SPC	3	ASPT-DIS	MICRO	U
IC	VLOC	CONSOLEA				U
IC	VLOC	CONSOLEB				U
CL	ASYNC-I/O	EIO-1	PU	A		C
			IC	CONSOLEA		U
CL	ASYNC-I/O	EIO-2	PU	A		C
			IC	CONSOLEB		U
MM	86-MEM	MB	KWD	4.8		U
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	CUM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CONFIGURATION

PROPOSED DEVICES TO COMPLEMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST
REPEAT REQUIRED COM LINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, --	OPTION 2, 5, 8, --	OPTION 3, 6, 9, --	CONTINUE
TYPE	DEVICE					
PU	XYZ32/75	A1	8	OS-XYZ-2B	FORTAN IV	C
			JOTAL 173	ASSEMBLER	FORTAN 73	U
PU	XYZ32/75	B1	3	OS-XYZ-2B	FORTAN IV	C
			JOTAL 173	ASSEMBLER		U
MM	32-MEM	M1	KWED	32		U
MM	32-MEM	M2	KWED	32		U
MM	32-MEM	M3	KWED	32		U
MM	32-MEM	M4	KWED	8		U
MM	32-MEM	M5	KWED	8		U
						U
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETICAL TECH DB

PROCESSOR: <u>NY232/75</u>		BYTE - <u>18</u> BITS		WORD - <u>18</u> BYTES									
OPERATING SYSTEM: <u>OS-MVP-28</u>		CYCLE TIME: <u>1.00</u> μ S/WORD		ACCESS TIME: <u>1.00</u> μ S/WORD									
MULTI TASK LEVEL: <u>64</u>		<table border="1"> <thead> <tr> <th>SIZE</th> <th>UNITS</th> </tr> </thead> <tbody> <tr> <td>K <u>6</u></td> <td>BYTES <u>WORDS</u></td> </tr> <tr> <td>K <u>8</u> M</td> <td>BYTES <u>WORDS</u></td> </tr> <tr> <td>K <u>9</u> M</td> <td>BYTES <u>WORDS</u></td> </tr> </tbody> </table>		SIZE	UNITS	K <u>6</u>	BYTES <u>WORDS</u>	K <u>8</u> M	BYTES <u>WORDS</u>	K <u>9</u> M	BYTES <u>WORDS</u>	LANGUAGES	
SIZE	UNITS												
K <u>6</u>	BYTES <u>WORDS</u>												
K <u>8</u> M	BYTES <u>WORDS</u>												
K <u>9</u> M	BYTES <u>WORDS</u>												
PRIORITY LEVEL: <u>64</u>		1. <u>ASSEMBLER</u> 2. <u>BASIC</u>											
ADDRESSABLE MEMORY: <u>4</u>		3. <u>FORTRAN IV</u> 4. <u>COBOL</u>											
OPERATING SYS. MEMORY: <u>48</u>		5. <u>ALGOL 68</u> 6. <u>MACRO-ASM</u>											
SUPPORT LIBRARY MEMORY: <u>20</u>		7. <u>FORTRAN 77</u> 8. <u></u>											
MULTI TASKING FEATURES AND RESOURCES													
LEVEL (1 to 1)	MAX TASKS	SERVICES P - PRIORITY S - SCHEDULING F - FILES	RESIDENT (R) NON-RESIDENT (NR) BATCH (B)	CIRCLE TYPES TIME SLAVE DATA	FREQUENCY TIMES/SECOND	OVERHEAD ENABLEMENT							
<u>1-54</u>		<u>E</u>	<u>R</u> NR S	<u>T</u> S D									
<u>55-63</u>		<u>E</u>	<u>R</u> <u>NR</u> S	<u>T</u> S D									
<u>64-64</u>		<u>E</u>	<u>R</u> NR <u>B</u>	<u>T</u> S D									
<u>ALL-255</u>		<u>L</u>	<u>R</u> NR S	<u>T</u> <u>B</u> <u>D</u>									
		<u>L</u>	<u>R</u> NR S	<u>T</u> S D									
		<u>L</u>	<u>R</u> NR S	<u>T</u> S D									
		<u>L</u>	<u>R</u> NR S	<u>T</u> S D									
		<u>L</u>	<u>R</u> NR S	<u>T</u> S D									
		<u>L</u>	<u>R</u> NR S	<u>T</u> S D									



BASILINE SOFTWARE APPLICATION IDENTIFICATION SAMPLE APPLICATION

DATA BLOCK DEFINITIONS

ID	LEVEL	DISCIPLINE	SYSTEM INTERFACE DEVICE	MAXIMUM RECORDS	MINIMUM		RECORD SIZE IN WORDS		
					BYTES/ BYTE	BYTES/ WORD	MINIMUM	AVERAGE	MAXIMUM
PAOL	5	RAN.	MM-M3	128	8	4	1	1	1
DIALITE	5	RAN.	MM-M3	256	8	4	1	1	1
CAMUT	6	CBMF	CL-HSD	2	8	4	128	128	128
ADASH	5	RAN.	CL-HSD	100	8	4	1	1	1
NOTPLIST	5	RAN.	CL-HSD	20	8	4	1	1	1
CALPT	5	CBMF	CL-HSD	2	8	4	128	128	128
RYADATA	5	RAN.	CL-HSD	8192	8	4	1	1	1
SIMPOS	6	CBMF	CL-FID-4	2	8	4	128	128	128
ANIMPOS	5	CBMF	MM-M1	2	8	4	128	128	128
GL	6	RAN.	U-_____	1024	8	4	1	1	1
ADDTA	6	RAN.	U-_____	512	8	4	1	1	1
ADDTA	6	RAN.	U-_____	512	8	4	1	1	1
ANIMETA	6	RAN.	U-_____	512	8	4	1	1	1
RYDATASH	5	RAN.	MM-M3	1	8	4	1	1	1
	U		U-_____	1					

SAMPLE PROBLEM MASTER BENCHMARK INSTRUCTION LIST

INSTRUCTION IDENTIFIER	BRIEF DESCRIPTION
AOI	- AREA OF INTEREST VISUAL COMPUTATIONS
BAOL	- BUILD ACTIVE OBJECT LIST
BLR	- BLINKING LIGHTS ROUTINE
BMBSTRAIMP	- BOMB STRAFE IMPACT TABLE ADJUSTMENT
BMPL	- BUILD MODEL PRIORITY LIST
CADCOSMAT	- COMPUTE CHANNEL ASSIGNMENT DIRECTIONAL COSINE MATRICES
CONIF	- VISUAL CONSOLE OPERATOR INTERFACE

Page 1 of 3

SAMPLE PROBLEM BENCHMARK INSTRUCTION LIST

INSTRUCTION IDENTIFER	BRIEF DESCRIPTION
DRLITADJ	- DIRECTIONAL LIGHT TABLE ADJUSTMENT
FADCOM	- FADING COMPUTATIONS
HOODDYN	- HOOD DYNAMICS
MMP	- MOVING MODEL PRIORITY
MMSADJ	- MOVING MODEL SITE ADJUSTMENT
PDYN	- PREPARE DYNAMIC DATA FOR OUTPUT
PEV	- PSEUDO EDGE VECTOR CALCULATION
RWV	- ROTATE WINDOW VECTORS
RWVM	- ROTATE WINDOW VECTORS MOVING MODEL

Page 2 of 3

SAMPLE PROBLEM MASTER BENCHMARK INSTRUCTION LIST

INSTRUCTION IDENTIFIER	BRIEF DESCRIPTION
	SHIPCAIPT - SHIP CHANNEL ASSIGNMENT INPUT DATA
SIMIF	- SIMULATOR MATH MODEL INTERFACE
TELV	- TERRAIN ELEVATION COMPUTATION
TSMMC	- TRANSFORM SUN VECTOR TO MOVING MODEL COORDINATES
T3	- SHIP POTENTIAL ACTIVE OBJECT LIST (PAOL) AND DIRECTIONAL LIGHT TABLE (DIRLITE)

Page 3 of 3

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETICAL TECH DB

INSTRUCTION BENCHMARK <u>HYPERMET</u>		ON PROCESSOR <u>80286/75</u>		USING _____ OPERATING SYSTEM	
BASIC STATEMENTS	SEMI BYTES USER CODE	STORES	TRANS CYCLES FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME PER OCCURRENCE
AVERAGE	<u>1200</u>	<u>20%</u>	<u>30%</u>	<u>40%</u>	<u>1</u> <u>20</u>
WORST CASE	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
LANGUAGE FACTORS:					
1 <u>FORTRAN 90</u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
2 <u>ALGOL 68</u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
3 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
4 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
5 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
6 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
7 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>
8 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u> <u> </u>

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

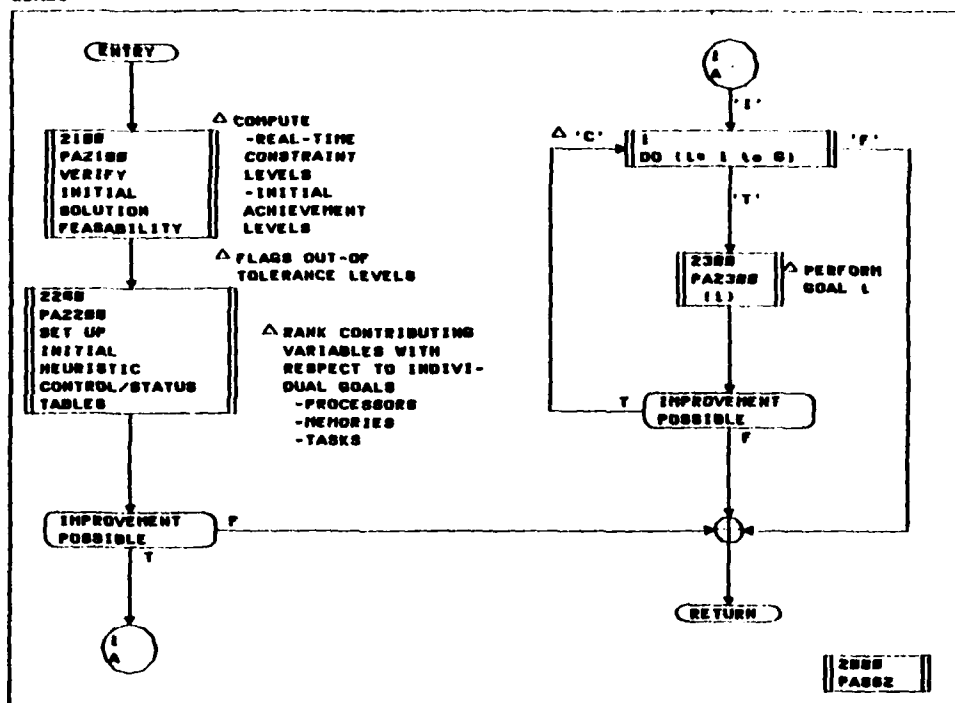
ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT	
			IDENTIFIER	VALUE IF APP.
U	T	T1-3	A1	30
T	T	T4-5	A1	30
L	T	A7-13	A1	30
L	T	T17-18	A1	30
B	T	T17-18	B1	30
T	T	B7-13	B1	30
T	T	T14216	B1	30
U	T	T15	B1	15
E	T	T15	A1	15

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT	
			IDENTIFIER	VALUE IF APP.
E	D	PAOL	M3	
E	D	DR.LITE	M3	
E	D	CADUTI	M4	
E	D	ADBJL	M3	
E	D	MOD.PLIST	M3	
E	D	CAIPT	M4	
E	D	DYNDATA	M3	
E	D	GI.MPOS	M1	
E	D	RAWPOS	M1	

DEALS



ISSUE DATE 15-NOV-79 ID DEALS SEC PFD-2000 PAGE 1

PROCESSOR LOAD BALANCE DEMO

PROBLEM: THREEFOLD BALANCE CHARACTERIZATION

- (1) NPGTL PROCESSORS OVER ABSOLUTE
UTILIZATION LIMIT**
- (2) NPGTG PROCESSORS ARE ABOVE GOAL
UTILIZATION**
- (3) (NP-NPGTG) PROCESSORS ARE AT OR
BELOW GOAL UTILIZATION**

PROCESSOR LOAD BALANCE DEMO

QUESTION POSED :

DOES AN IMPROVED ALLOCATION EXIST?

**I.E. CAN THE PROCESSORS BELOW GOAL
UTILIZATION PERFORM SOME OF THE TASKS
CURRENTLY ALLOCATED TO HEAVILY
UTILIZED PROCESSORS?**

PROCESSOR LOAD BALANCE DEMO

ALGORITHM SOLUTION TECHNIQUE

- RANK PROCESSOR UTILIZATION U_p WITH RESPECT TO GOAL G_p USING $(G_p - U_p)$ AS MEASUREMENT
- IF $U_p > L_p$ (ABSOLUTE LIMIT EXCEEDED) ADD A LARGE NEGATIVE PENALTY TO DIFFERENCE
- RANK RESULTING DIFFERENCES IN DESCENDING ORDER
NOTE: LEAST LOADED PROCESSORS WILL APPEAR FIRST
- ATTEMPT TO OFFLOAD PROCESSOR ABOVE LIMIT
- SEE IF LEAST LOADED PROCESSOR CAN RELIEVE ANY OF THE HEAVILY LOADED PROCESSORS

PROCESSOR LOAD BALANCE DEMO

SAMPLE PROBLEM INPUTS

PROCESSOR	COMPONENT TASK	UTIL	U_p	G_p	L_p	$U_p^1 - G_p - U_p$
1	1	50	100	60	75	-140*
	2	10				
	3	25				
	4	15				
2	5	40	40	40	75	0
3	6	20	20	60	75	+40

* PENALTY FOR BEING OVER ABSOLUTE LIMIT = 100

PROCESSOR LOAD BALANCE DEMO

SAMPLE PROBLEM TEST CASES

CASE	DESCRIPTION	RESULTS	
		PROC-TASKS	UTILIZATION
1	IDENTICAL PROCESSORS SHARED MEMORY ALL BLOCKS	P1-T1, T2 P2-T5 P3-T6, T3, T4	60 40 60
2	IDENTICAL PROCESSORS SHARED MEMORY DATA BLOCKS PRIVATE MEMORY INSTRUCTION BLOCKS	P1-T1, T2 P2-T5 P3-T6, T3, T4	60 40 60
3	IDENTICAL PROCESSORS SHARED MEMORY DATA BLOCKS PRIVATE MEMORY INSTRUCTION BLOCKS T3 FIXED ON P1, T1 PROHIBITED ON P3	P1-T1, T3 P2-T5 P3-T6, T4, T2	75* 40 45

*ABOVE GOAL UNABLE TO OFFLOAD

```

graph TD
    ENTRY([ENTRY]) --> I1([1])
    I1 --> F1{ }
    F1 -- F --> I2([2])
    F1 -- T --> N0[N=0]
    N0 --> I3([1])
    I3 --> P1[PROCESS EACH PROCESSOR  
J ABOVE ABSOLUTE LIMIT]
    P1 --> I4([1])
    I4 --> DO[DO (for I  
= 1 to NPLTL)]
    DO --> J1[J=CDPCD[NP-L+1]  
J1=NP-NPSTS+1]
    J1 --> Z321[Z321  
FACTSK  
(J, IJT, IJLIST)]
    Z321 --> I5[IJT, LE, 0]
    I5 -- F --> I6([3])
    I5 -- T --> P2[100  
PERROR  
(43)]
    P2 --> I7([1])
    I7 --> I8([1])
    I8 --> J2[J1=NP-NPSTS+1]
    J2 --> Z21[Z21  
IRANKD  
(CDPCD, CDPCD1, I, J1)]
    Z21 --> I9([C])
    I9 --> DO
    I9 --> R1[REARRANGE  
PROCESSORS  
WHICH ARE  
LESS THAN  
OR EQUAL GOAL]
    R1 --> I10([3])
    I10 --> I4
  
```

2320
LOADBL

ENTRY

1

2

SOME PROCESSORS
ARE ABOVE LIMIT

N=0

1

PROCESS EACH PROCESSOR
J ABOVE ABSOLUTE LIMIT

1

DO (for I
= 1 to NPLTL)

J=CDPCD[NP-L+1]
J1=NP-NPSTS+1

Z321
FACTSK
(J, IJT, IJLIST)

IJT, LE, 0

3

100
PERROR
(43)

FIXED
ALLOCATION
HAS OVERLOADED
PROCESSOR J

1

1

J1=NP-NPSTS+1

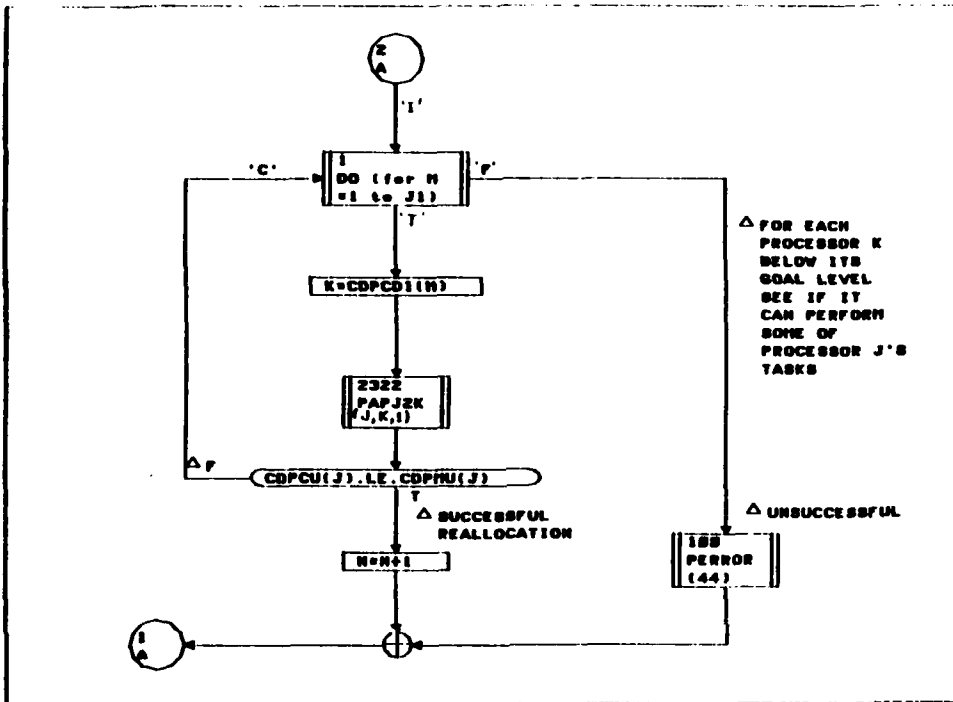
Z21
IRANKD
(CDPCD, CDPCD1, I, J1)

C

REARRANGE
PROCESSORS
WHICH ARE
LESS THAN
OR EQUAL GOAL

3

DEALS



1 RUE

DATE 19-NOV-79

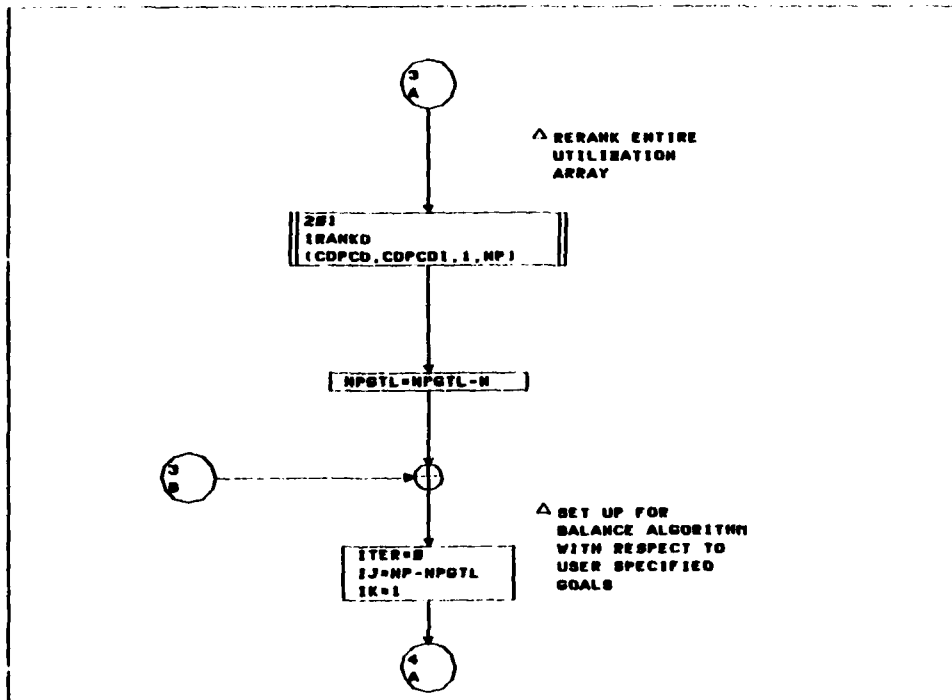
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SEC PPD-232B

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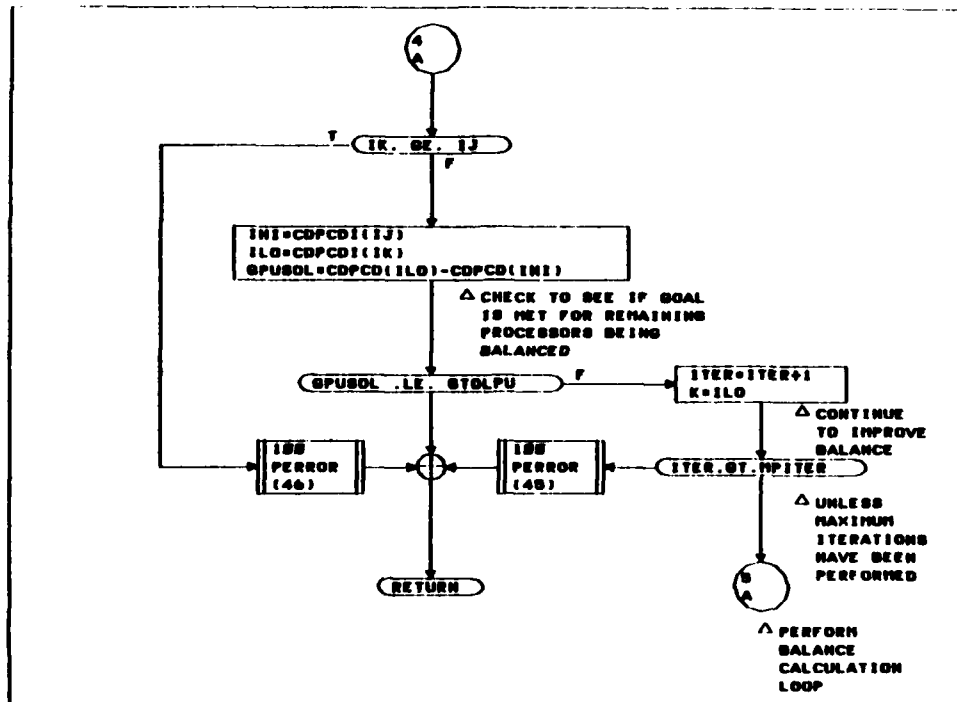
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DEALS



ISSUE DATE 19-NOV-79 10 DEALS SEC PPD-2328 PAGE 3

DEALS



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DATE 19-NOV-79

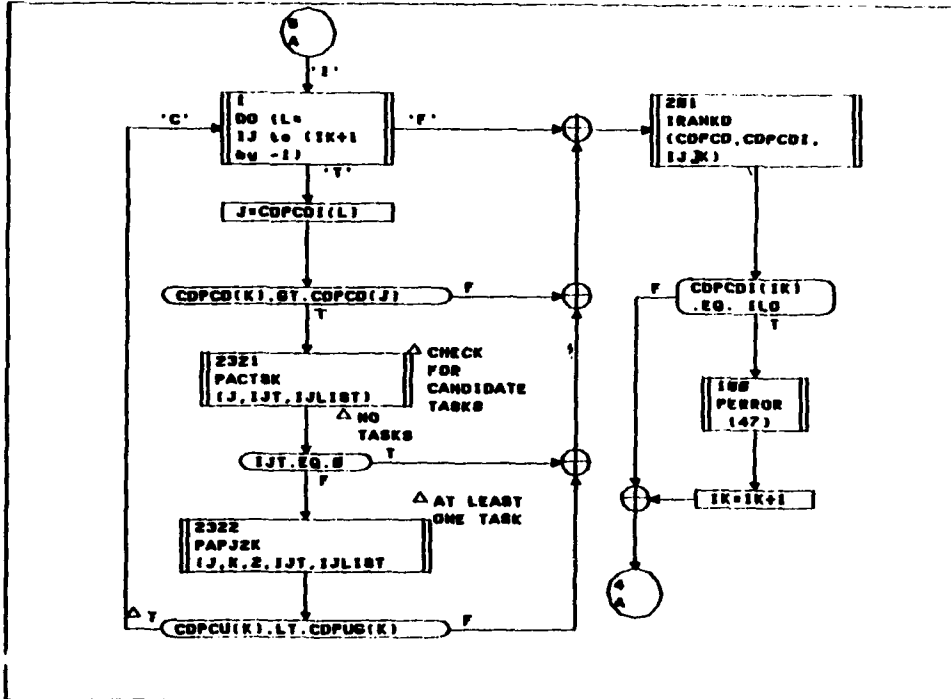
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SEC PFD-2328

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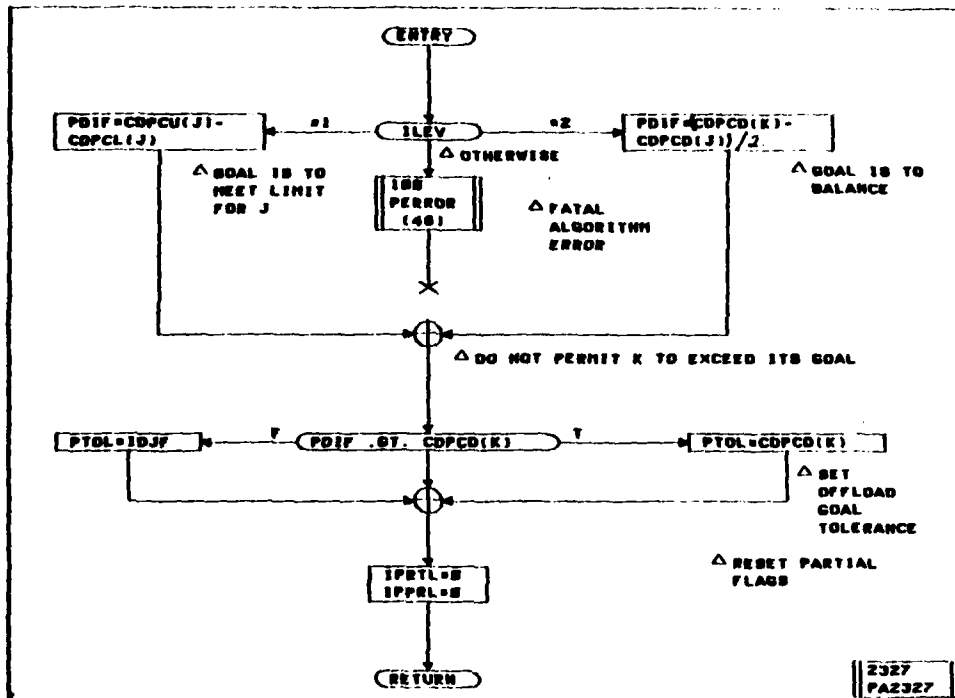
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DEALS



ISSUE DATE 28-NOV-79 ID DEALS SEC PPD-2326 PAGE 5

DEALS



ISSUE

DATE 28-NOV-79

10 DEALS

SEC PPD-2327

PAGE 1

2327
PA2327

MEMORY ALLOCATION BALANCE DEMO

PROBLEM : THREEFOLD BALANCE CHARACTERIZATION

- (1) NMGTL MEMORIES ARE ABOVE ABSOLUTE LIMIT**
- (2) NMGTG MEMORIES ARE ABOVE GOAL UTILIZATION**
- (3) (NM-NMGTG) MEMORIES ARE AT OR BELOW GOAL
UTILIZATION**

MEMORY ALLOCATION BALANCE DEMO

QUESTION POSED :

DOES AN IMPROVED ALLOCATION EXIST?

**I.E. CAN THE MEMORIES BELOW GOAL ALLOCATIONS
BE ASSIGNED DATA / INSTRUCTION BLOCKS FROM
OVER ALLOCATED MEMORIES?**

MEMORY ALLOCATION BALANCE DEMO

SOLUTION TECHNIQUE

- RANK MEMORY ALLOCATIONS u_m WITH RESPECT TO GOAL q_m
USING $(q_m - u_m)$ AS MEASUREMENT
- MEMORY HEURISTIC CONTROL FLOW IDENTICAL TO PROCESSOR
LOAD BALANCE HEURISTIC WITH
 - BLOCKS IN PLACE OF TASKS
 - MEMORIES IN PLACE OF PROCESSORS
- DETAILED CALCULATIONS DIFFER SIGNIFICANTLY

MEMORY ALLOCATION BALANCE DEMO

SAMPLE PROBLEM INPUTS

MEMORY	COMPONENT BLOCK	UTIL	U_m	G_m	L_m	$U'_m - G_m - U_m$
1	1	10	80	60	70	-120*
	2	30				
	3	40				
2	4	20	20	60	70	+40

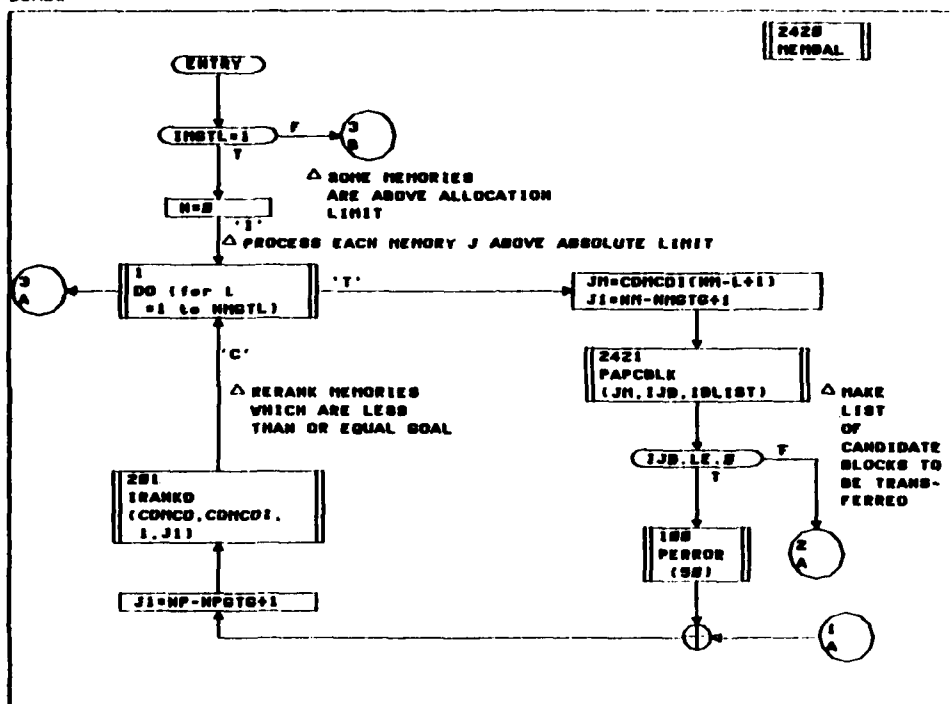
*PENALTY FOR BEING OVER ABSOLUTE LIMIT = /100

MEMORY ALLOCATION BALANCE DEMO

SAMPLE PROBLEM TEST CASES

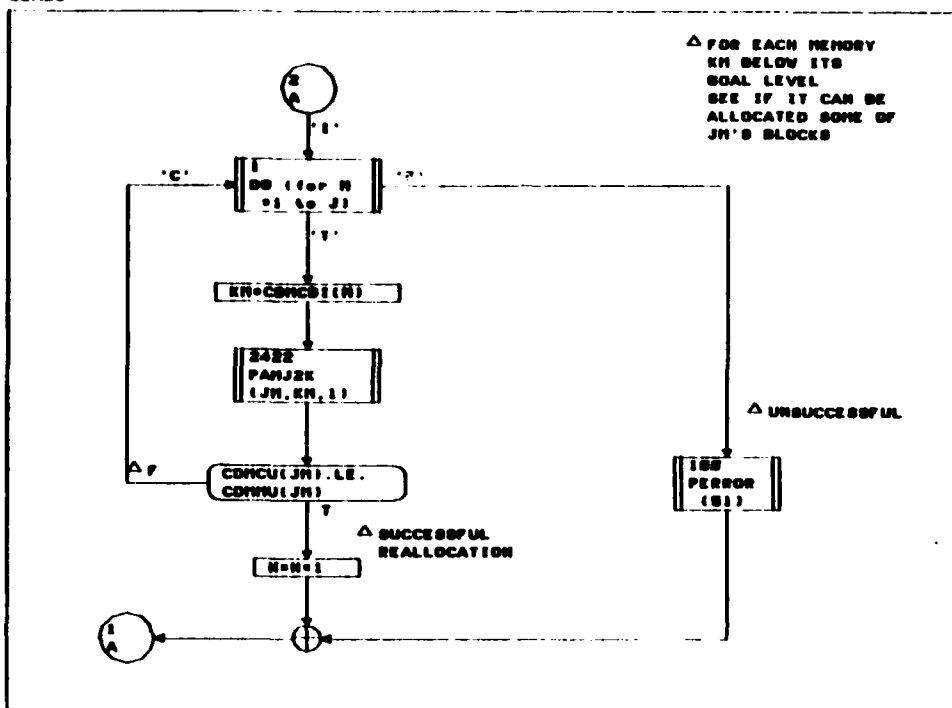
CASE	DESCRIPTION	RESULTS	
		MEMORY-BLOCKS	UTILIZATION
1	BOTH MEMORIES AVAILABLE TO ALL PROCESSORS IDENTICAL MEMORIES	M1 - B3, B1 M2 - B2, B2	50 50
2a	SAME AS CASE 1 EXCEPT B2 FIXED ON M1 WITHOUT SWAP	M1 - B2, B3 M2 - B4, B1	70 30
2b	SAME AS CASE 2a EXCEPT SWAP ALGORITHM ADDED	M1 - B2, B4 M2 - B3, B1	50 50
3a	M2 REQUIRES DOUBLE SPACE TO STORE BLOCK 1 AND NO FIXED ASSIGNMENTS NO SWAP	M1 - B2, B3 M2 - B4, B1	70 40
3b	SAME AS CASE 3a EXCEPT SWAP ALGORITHM ADDED	M1 - B1, B3 M2 - B4, B2	50 50

DEALS



ISSUE DATE 26-NOV-79 ID DEALS SEC PPD-2420 PAGE 1

DEALS



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DATE 26-NOV-79

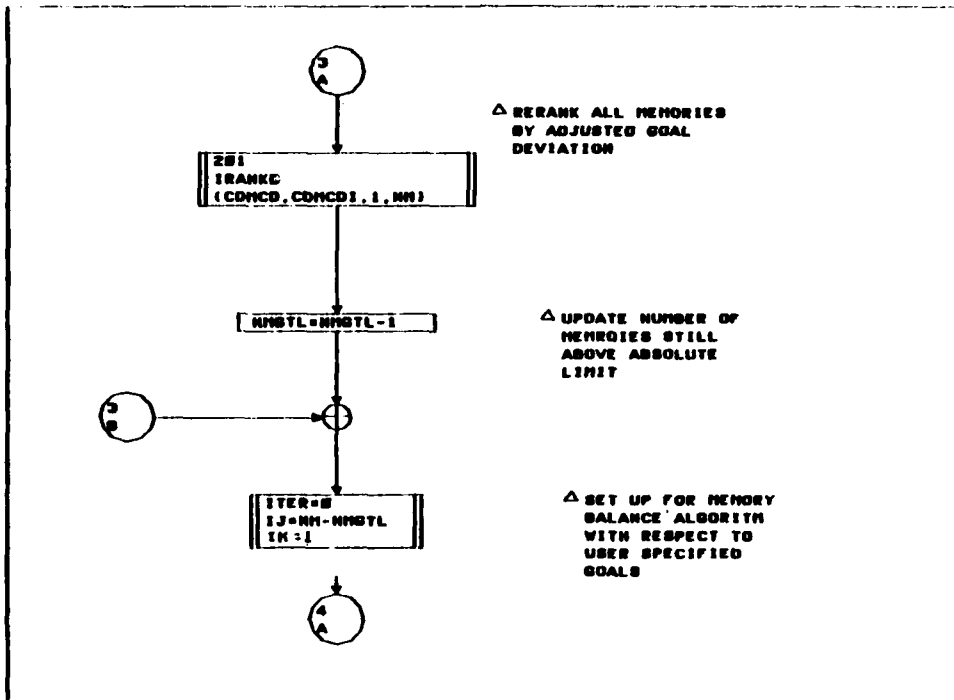
ID DEALS

SEC PPD-2428

PAGE

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DEALS



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26-NOV-79

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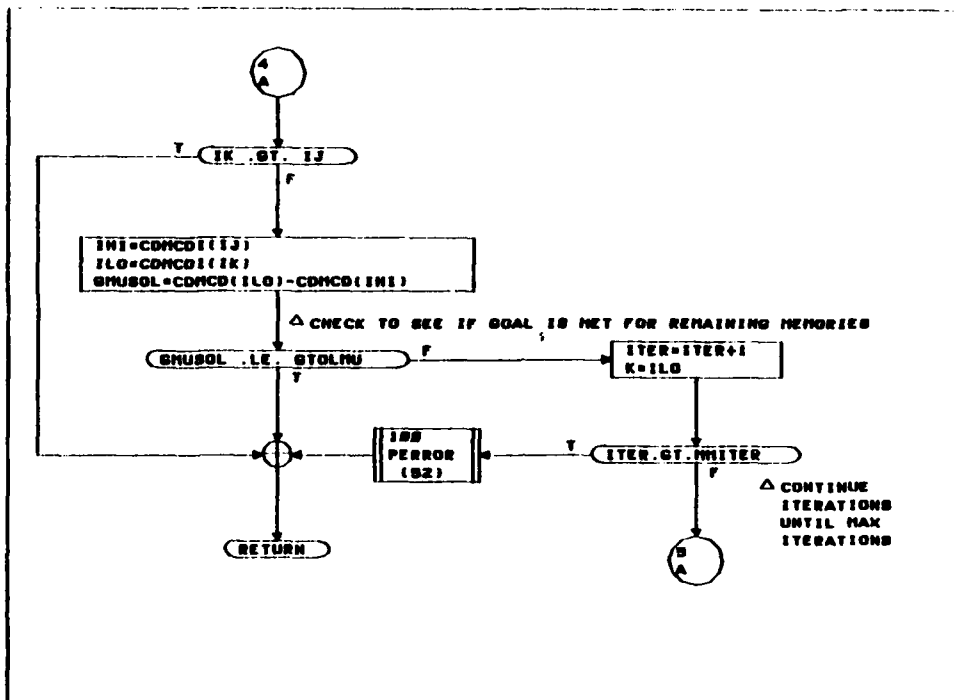
DEALS

SEC PPD-2428

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DEALS



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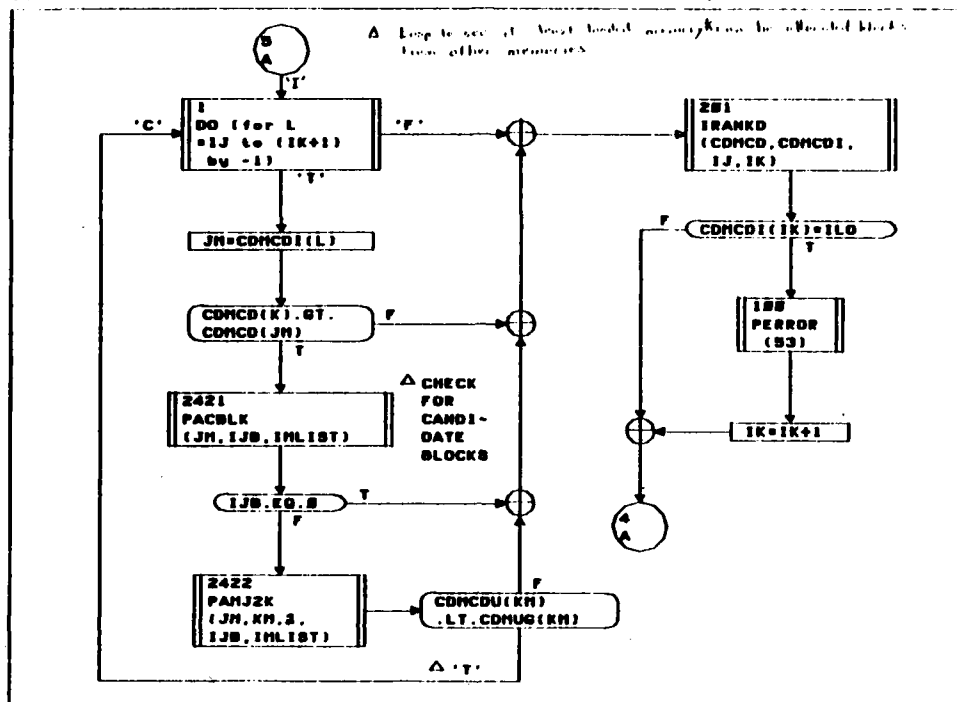
ID DEALS

SEC PPD-242B

PAGE

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DEALS



ISSUE

DATE 26-NOV-79

ID DEALS

SEC PPD-2428 PAGE

8

REDUCE DEVELOPMENT COST DEMO

PROBLEM AREAS:

- (1) HOMOGENEOUS VERSUS HETEROGENEOUS CANDIDATE
CONFIGURATION COMPONENTS**
- (2) EXISTING VERSUS NEW SOFTWARE / FIRMWARE
CAPABILITIES**
- (3) SOURCE OF GOOD INPUT ESTIMATES FOR A GIVEN
ALLOCATION**

REDUCE DEVELOPMENT COST DEMO

QUESTIONS POSED FOR HOMOGENEOUS CASE

- (1) CAN A MORE COST EFFECTIVE DEVELOPMENT LANGUAGE
BE USED FOR DEVELOPMENT AND STILL MEET REAL-TIME
CONSTRAINTS?**
- (2) IF A TASK IS CURRENTLY ALLOCATED TO MORE THAN ONE
PROCESSORS CAN THE NUMBER OF PROCESSORS BE
REDUCED AND WHAT IMPACT DOES THIS HAVE ON
DEVELOPMENT COST?**

REDUCE DEVELOPMENT COST DEMO

QUESTIONS POSED FOR HETEROGENEOUS CASE

- (1) ARE ANY TASKS ASSIGNED TO PROCESSORS OF DIFFERENT TYPES?**
- (2) IF SO, CAN A HOMOGENEOUS ASSIGNMENT BE FOUND FOR THEN TASK ALLOCATION?**

REDUCE DEVELOPMENT COST DEMO

ALGORITHM TECHNIQUES

- 1. DO NOT PERMIT PARTIAL ALLOCATIONS OF TASKS TO HETEROGENEOUS PROCESSORS IN LOADBL UNLESS PRESET CONSTRAINT.**
- 2. DO NOT PERMIT DUPLICATE BLOCKS ON HETEROGENEOUS MEMORIES IN MEMBAL.**
- 3. CREATE A TASK ALLOCATION CHANGE LIST OF TASKS WHICH COULD BE SWAPPED TO REDUCE DEVELOP COST AND STILL MEET REAL-TIME CONSTRAINTS.**
- 4. PROCESS CHANGE LIST TO SEE IF TASK EXCHANGES CAN BE MADE BETWEEN A GIVEN PAIR OF PROCESSORS.**

REDUCE DEVELOPMENT COST DEMO

TEST CASES

CASE	TASK	PROC1 D. C.	PROC2 D. C.
BASIC INPUTS	T1	5	3
	T2	2	4
CASE 1 SWAP CONDITION	T1	✓	
	T2		✓
CASE 2 REDUCE PROCESSOR CONDITION	T1	✓	✓
	T2	✓	✓

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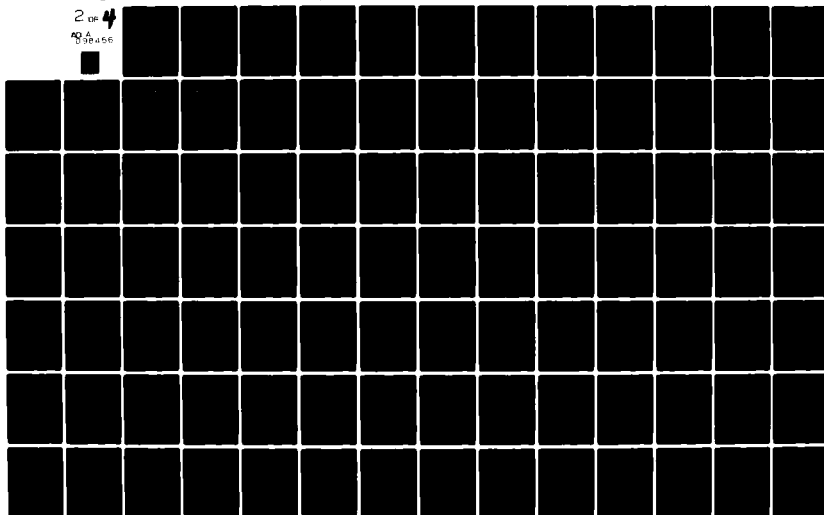
TELEDYNE BROWN ENGINEERING HUNTSVILLE ALA SYSTEMS DIV F/6 9/2
SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
FEB 81 S J CLYMER F33615-78-C-0013

UNCLASSIFIED

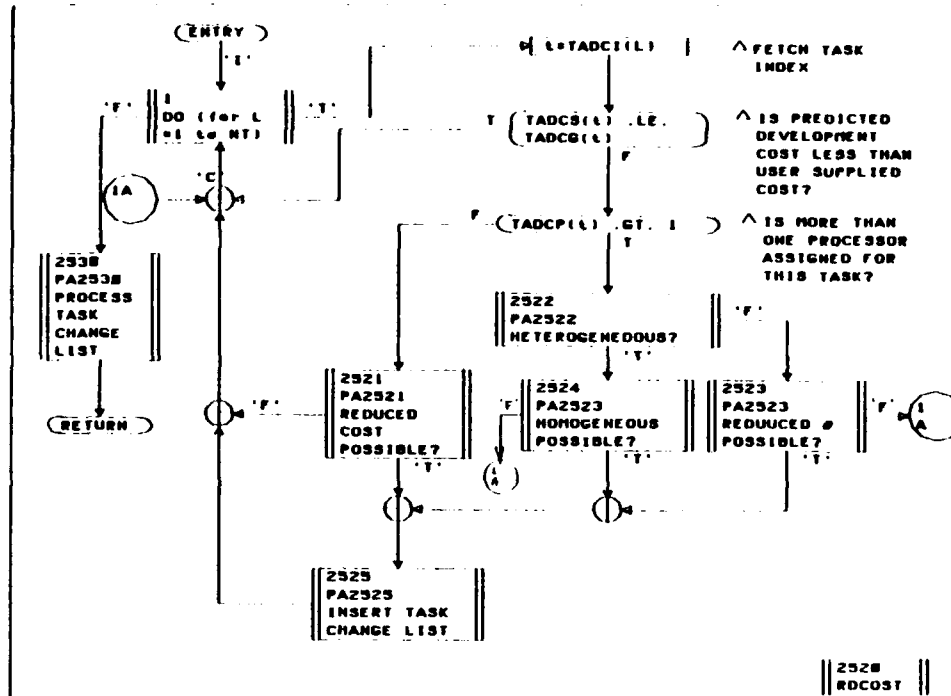
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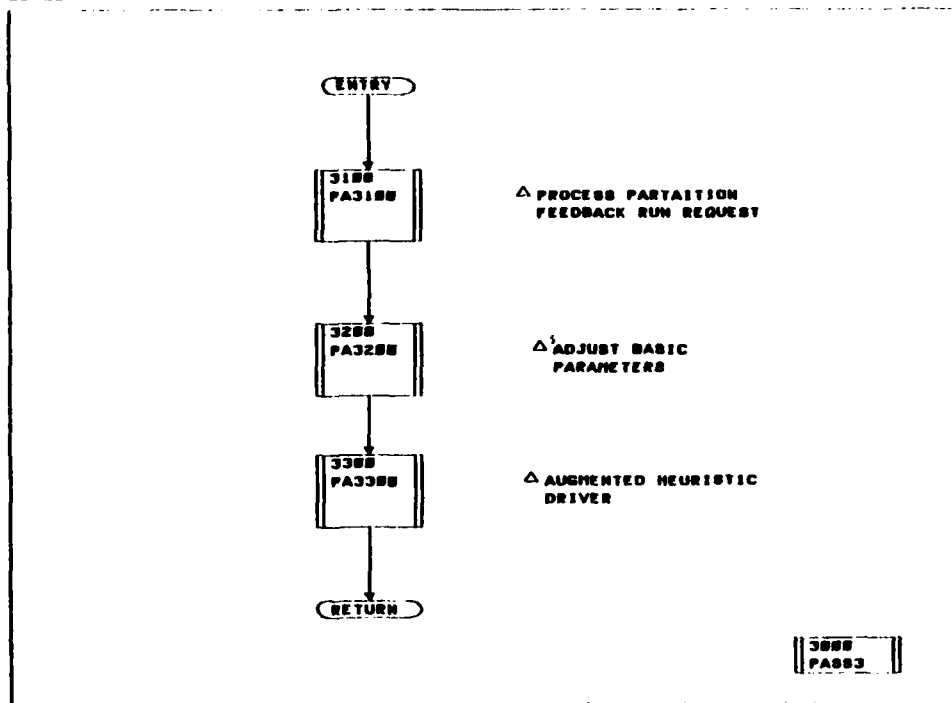
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DATE 18-DEC-79 ID DEALS

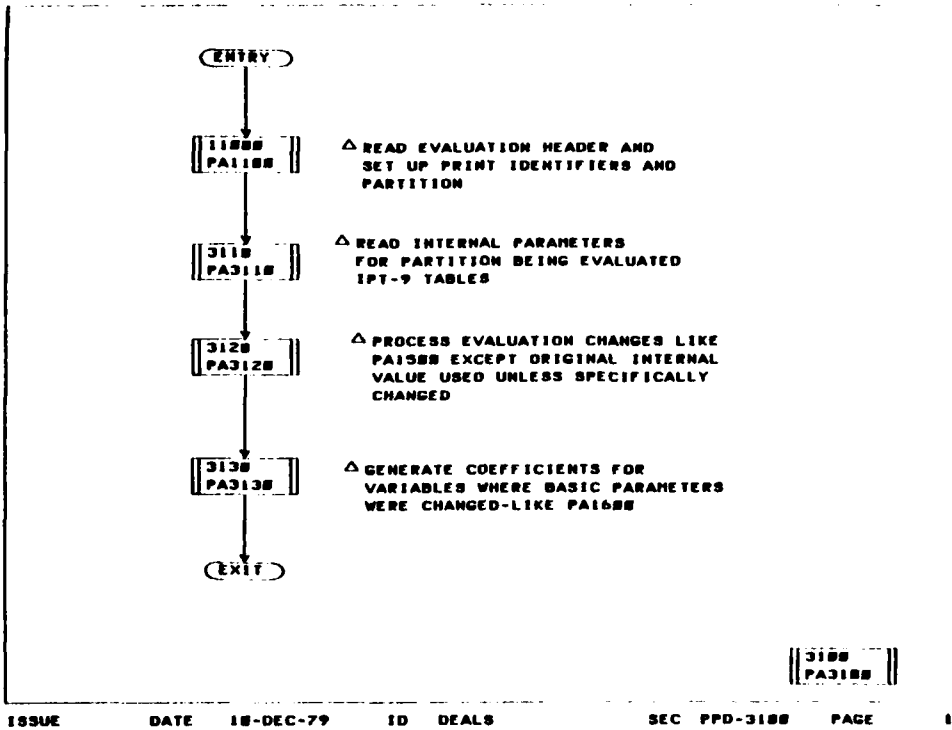
SEC PDB-2528 PAGE 1

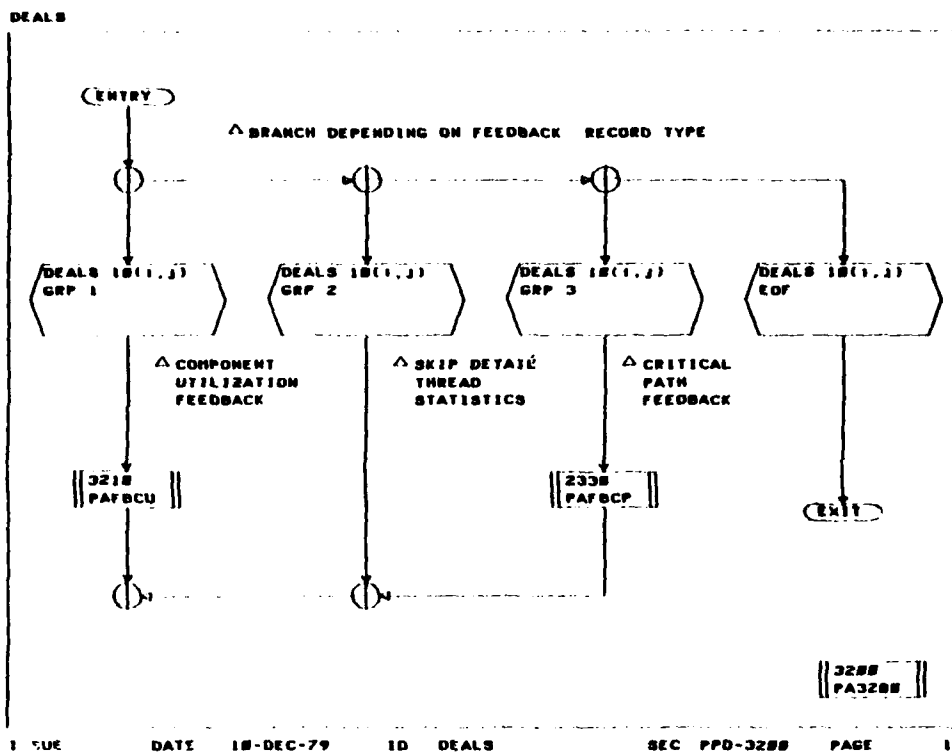
DEALS



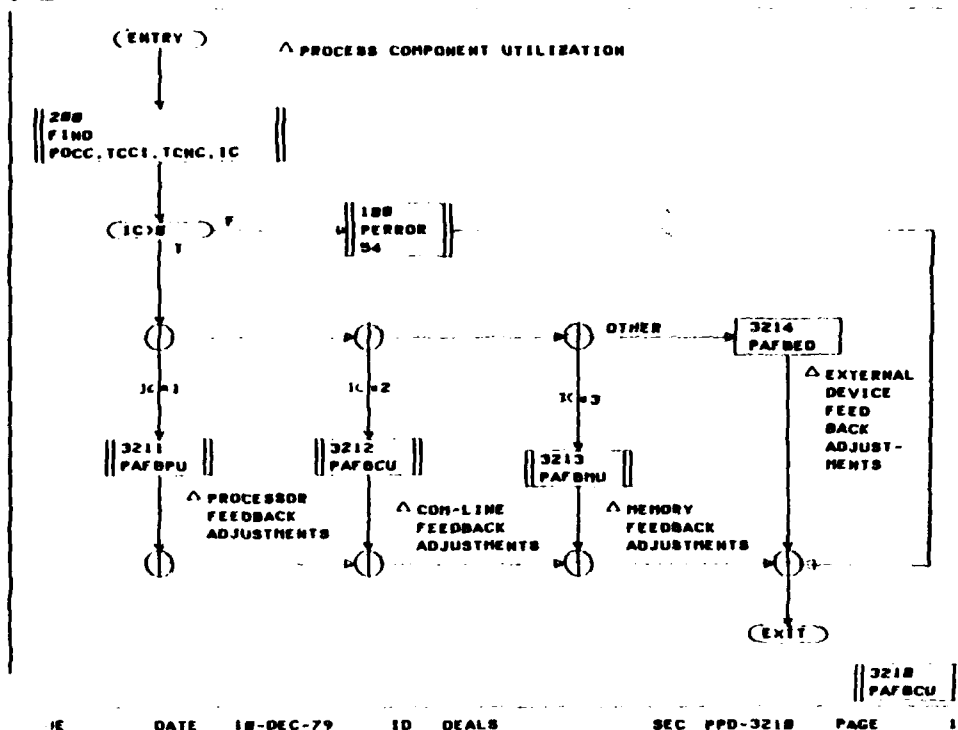
ISSUE DATE 28-NOV-79 ID DEALS SEC PPU-3000 PAGE 1

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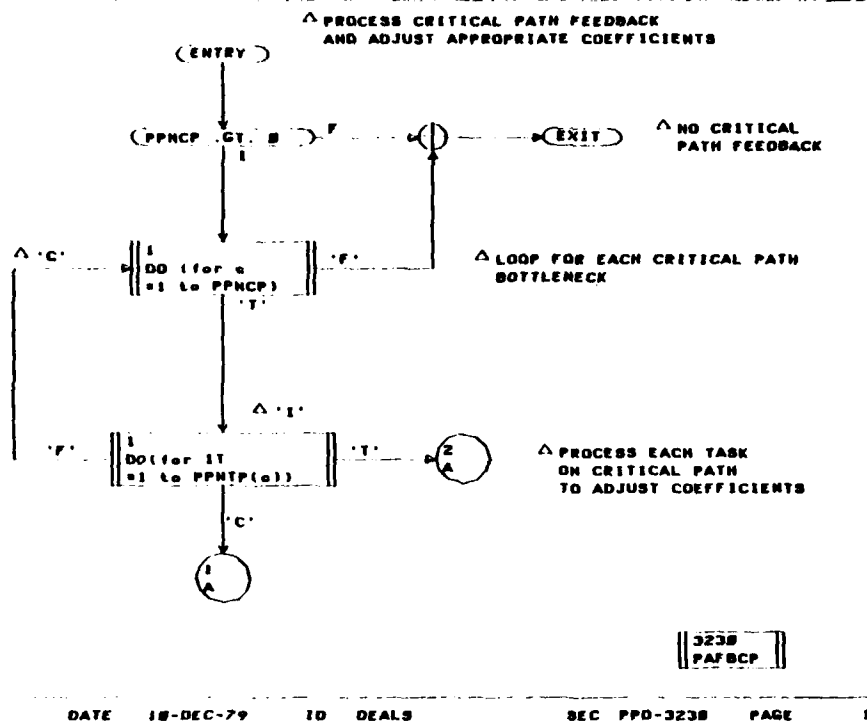




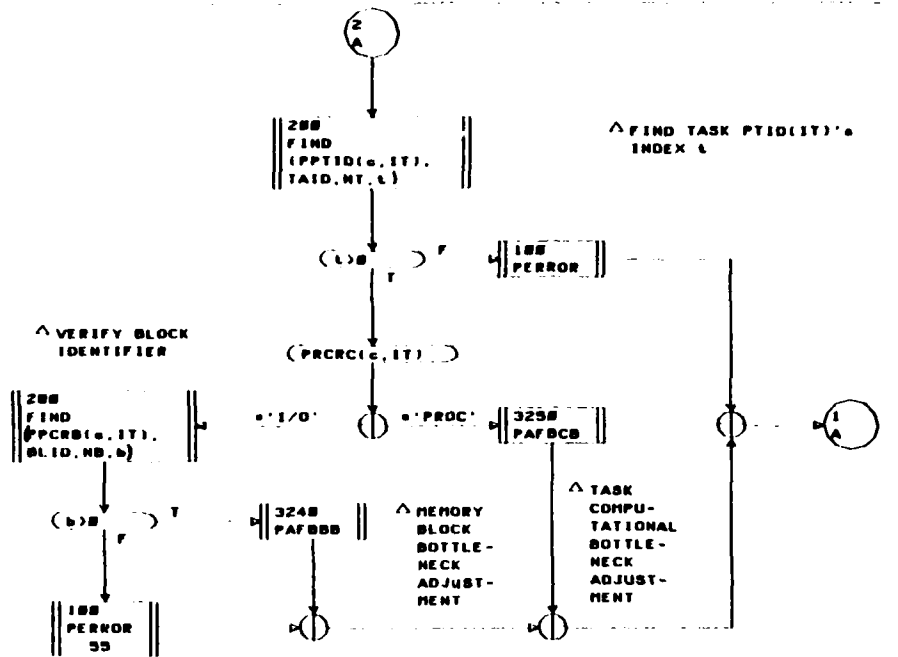
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REPORT GENERATOR DEMO

PURPOSE : TO PRESENT PARTITION SOLUTION
FOR USER EVALUATION AND ANALYSIS

PROBLEM : DIFFERENT USERS HAVE DIFFERENT NEEDS

SOLUTION : FLEXIBLE REPORT GENERATOR DESIGN

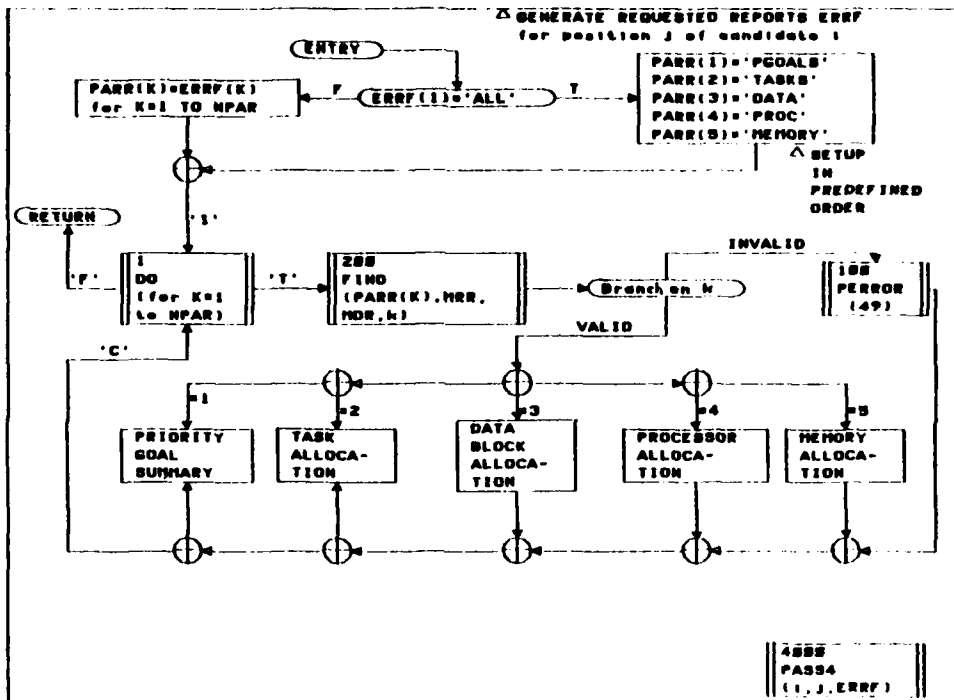
- MAINTENANCE OF A MASTER SET OF REPORTS
- USER SELECTED AND ORDERED REPORT
GENERATION

REPORT GENERATOR DEMO

FEASIBILITY ISSUES

- **SOLUTION DATA BASE FORMAT**
 - **NUMBER OF PARTITIONS SAVED**
 - **MULTIPLE FILES WITH REORDERED RECORDS
VERSUS TEMPORARY FILE SORTS AND/OR
CROSS INDEXED LINKED LISTS**
- **HARDCOPY VERSUS INTERACTIVE DISPLAY**

DEALS



ISSUE

DATE

28-NOV-79

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DEALS

SEC PDB-40PM

PAGE

1

REPORT GENERATOR DEMO

INITIAL MASTER REPORT FORMATS

- **PRIORITY GOAL SUMMARY**
- **TASK ALLOCATION**
- **DATA BLOCK ALLOCATION**
- **PROCESSOR ALLOCATION**
- **MEMORY ALLOCATION**

PRIORITY GOAL SUMMARY DEMO

PURPOSE : TO PROVIDE MAJOR PARTITION
MEASUREMENTS IN TERMS OF
EVALUATION GOALS AND
PRIORITIES

PROBLEM : CLEARLY IDENTIFY PRIORITIES,
UNITS OF MEASURE, TOLERANCES,
LEVEL OF ACHIEVEMENT, AND
CONTRIBUTING COMPONENTS FOR
A GIVEN PARTITION ALLOCATION

TASK ALLOCATION DEMO

PURPOSE : TO PROVIDE PARTITION ALLOCATION
OF EACH TASK IN TERMS OF ASSIGNED
PROCESSORS AND TASK I/O BLOCK
MEMORY SOURCES

PROCESSOR ALLOCATION SUMMARY DEMO

**PURPOSE : TO SUMMARIZE PROCESSOR ALLOCATION
VIA ASSIGNED TASK MIX AND
UTILIZATION PARAMETERS**

DATA BLOCK ALLOCATION SUMMARY DEMO

PURPOSE : TO PROVIDE MAPPING OF EACH DATA
BLOCK AS ALLOCATED TO MEMORIES
OF CANDIDATE CONFIGURATION AND
CROSS REFERENCE TO PROCESSOR
COMMUNICATIONS

MEMORY ALLOCATION SUMMARY DEMO

**PURPOSE: TO SUMMARIZE MEMORY ALLOCATION
VIA ASSIGNED DATA BLOCK MIX AND
UTILIZATION PARAMETERS**

C.2 SAMPLE INPUTS

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX.
 PARTITION NUMBER 1110

FILE	IDENTIFIER
COMPUTATIONAL INTERFACE REQUIREMENTS	INTERFACE DEFINITION
BASELINE APPLICATION COMPONENTS	SAMPLE APPLICATION
CANDIDATE CONFIGURATION COMPONENTS	SAMPLE CONFIGURATION
BASELINE PARTITIONING LOAD	GLOBAL LOAD EXAMPLE
TECHNOLOGY DATA BASE	HYPOTHETICAL TECH.DB

EVALUATION RUN IDENTIFIER GLOBAL PARTITION EX

GLOBAL EVALUATION FACTORS

PRIORITY	ORDER	GOAL	UPPER LIMIT	COEFFICIENT LEVELS	MAXIMUM ITERATIONS
PROCESSOR UTILIZATION (% BUSY)	1	40.0	60.0	AVERAGE WORST CASE	10
MEMORY UTILIZATION (% OCCUPIED)	2	40	60.00	AVERAGE WORST CASE	10
DEVELOPMENT COST (PERSON YEARS)	3	3	4.5	AVERAGE WORST CASE	5

COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS FILE IDENTIFIER INTERFACE DEFINITION

REQUIRED COMPONENTS

TYPE	COMPONENT		UNIQUE SYSTEM IDENTIFIER	OPTION 1, 4, 7, --	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
	DEVICE						
PU	86-PROC		A		CUSTOM-VLS	ASSEMBLER	G
					MON-AS-M		
PA	SPC		SPC		ASPT-DIS	MICRO	
IC	VIOC		CONSOLEA				
IS	VIOC		CONSOLEB				
CL	ASNG-IO		EIO-1		A		G
					CONSOLEA		
CL	ASNG-IO		EIO-2		A		G
					CONSOLEB		
MM	86-MEM		MM				
					48		
PU	PROCESSOR DEVICE			1. ACTIVE LEVELS 4. LANGUAGE 2	2. OPERATING SYSTEM 5. LANGUAGE 3	3. LANGUAGE 1 6. LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE			1. SIZING UNIT	2. SIZE		
CL	COM DEVICE			INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

COMPUTATIONAL SUBSYSTEM INTERFACE REQUIREMENTS FILE IDENTIFIER INTERFACE DEFINITION

REQUIRED COMPONENTS

COMPONENT		UNIQUE SYSTEM IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
CU	ATLHk-26a	EIO-3	PU	A		S
			PU	SPC		
CU	HSD	EIO-4				
PU	PROCESSOR DEVICE		1. ACTIVE LEVELS 4. LANGUAGE 2	2. OPERATING SYSTEM 5. LANGUAGE 3	3. LANGUAGE 1 6. LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1. SIZING UNIT	2. SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CANDIDATE IDENTIFIER

PROPOSED DEVICES TO COMPLEMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST

REPEAT REQUIRED COMBINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
PU	XYZ32/75	A1	8	OS-XYZ-2R	FORTRAN IV	C
			10VIAL-173	ASSEMBLER	FORTRAN 7D	
PU	XYZ32/75	B1	3	OS-XYZ-2R	FORTRAN IV	C
			10VIAL-173	ASSEMBLER		
MM	32-MEM	M1	8WED	32		
MM	32-MEM	M2	8WED	32		
MM	32-MEM	M3	8WED	32		
MM	32-MEM	M4	8WED	8		
MM	32-MEM	M5	8WED	8		
PU	PROCESSOR DEVICE		1. ACTIVE LEVELS 4. LANGUAGE 2	2. OPERATING SYSTEM 6. LANGUAGE 3	3. LANGUAGE 1 8. LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1. SIZING UNIT	2. SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

CANDIDATE CONFIGURATION IDENTIFIER SNAPL-CONF-1587-0001

PROPOSED DEVICES TO COMPLIMENT REQUIRED DEVICES
LIST COMMUNICATION LINES LAST
REPEAT REQUIRED COMLINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
CU	MBUS	C1	PU	A1		G
			MM	A1		
CU	MBUS	C2	PU	B1		C
			MM	M2		
CU	MBUS	BUS2	PU	A1		G
			PU	B1		G
			MM	M3		
CU	MBUS	BUS1A	PU	C1		G
			MM	M4		
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

NOT ANALYZED TO RDS

10-1-76
 10-1-76
 10-1-76

CANDIDATE CONFIGURATION IDENTIFIER SAMPLE CONTINUATION

PROPOSED DEVICES TO COMPLEMENT REQUIRED DEVICES
 LIST COMMUNICATION LINES LAST
 REPEAT REQUIRED CONLINES IF ADDITIONAL DEVICES ARE INTERFACED

COMPONENT		CANDIDATE IDENTIFIER	OPTION 1, 4, 7, ...	OPTION 2, 5, 8, ...	OPTION 3, 6, 9, ...	CONTINUE
TYPE	DEVICE					
CU	MBUS	BUS1B	PU	AL		C
U			MM	M5		U
CU	HSD	HSD	PU	AL		C
U			PU	A		U
CU	86MBUS	BUS3	PU	A		U
U			MM	M6		U
CU	HSD	ETD-4	PU	AL		U
U						U
U						U
U						U
PU	PROCESSOR DEVICE		1 - ACTIVE LEVELS 4 - LANGUAGE 2	2 - OPERATING SYSTEM 5 - LANGUAGE 3	3 - LANGUAGE 1 6 - LANGUAGE 4	CONTINUE IF MORE LANGUAGES ARE SPECIFIED
MM	MEMORY DEVICE		1 - SIZING UNIT	2 - SIZE		
CL	COM DEVICE		INTERFACING DEVICE TYPE	INTERFACING COMPONENT	PRIORITY	CONTINUE IF MORE INTERFACING DEVICES

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

PROCESSOR: <u>8232/75</u>		BYTE - <u>16</u> BITS		WORD - <u>16</u> BYTES	
OPERATING SYSTEM: <u>OS-XVZ-28</u>		CYCLE TIME: <u>0.00</u> μ SWORD		ACCESS TIME: _____	
MULTI TASK LEVELS: <u>64</u>		SIZING		LANGUAGES	
PRIORITY LEVELS: <u>64</u>		K <u>64</u>		1. ASSEMBLY BASIC	
ADDRESSABLE MEMORY: _____		M <u>64</u>		2. FORTRAN IV COBOL	
OPERATING SYS. MEMORY: <u>48</u>		M <u>64</u>		3. DOLAN-173 MACRO-ASM	
SUPPORT LIBRARY MEMORY: <u>28</u>		M <u>64</u>		4. FORTRAN 77	

LEVEL	MAX TASKS	SERVICED P - PRIORITY S - SCHED F - FIFO	MULTI TASKING FEATURES AND RESOURCES		ENABLERMENT RESOURCE MANAGEMENT	
			RESIDENT (R) NON-RESIDENT (NR) HATCH (H)	CIRCLE TYPE (C) TIME SLAVE DATA	ENLIGHTENED TIME SCHEDULE	ONLINE ENLIGHTENMENT
<u>54</u>		<u>15</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
<u>55</u>		<u>5</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
<u>64</u>		<u>5</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
<u>ALL</u>	<u>255</u>	<u>1</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
		<u>1</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
		<u>1</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
		<u>1</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		
		<u>1</u>	<u>R</u> NR <u>B</u>	<u>T</u> S <u>D</u>		

THIS PAGE IS BEST QUALITY
FROM GOVERNMENT DOCUMENTS

331/Jan 1973

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

PROCESSOR: <u>86-PAC</u>		BYTE = <u> </u> BITS	WORD = <u> </u> BYTES
OPERATING SYSTEM: <u>CUSTOM-VLS</u>		CYCLE TIME: <u> </u> μ S/WORD	ACCESS TIME: <u> </u> μ S/WORD
MULTI TASK LEVELS: <u> </u>		LANGUAGES	
PRIORITY LEVELS: <u> </u>		1 <u>ASSUMER</u> 5 <u> </u>	
ADDRESSABLE MEMORY: <u> </u>		2 <u>FORTRAN IV</u> 6 <u> </u>	
OPERATING SYS. MEMORY: <u> </u>		3 <u>MARCA-ASM</u> 7 <u> </u>	
SUPPORT LIBRARY MEMORY: <u> </u>		4 <u> </u> 8 <u> </u>	

LEVEL (1-10)	MAX TASKS	MULTI TASKING FEATURES AND RESOURCES				ENABLEMENT RESOURCE MANAGEMENT	
		SERVICED P - PRIORITY F - FIFTH F - FIFTH	RESIDENT (R) NON-RESIDENT (NR) BATCH (B)	CIRCLE TYPE TIME SLAVE DATA	FREQUENCY TIMES/COND	OUT/HEAD/ENABLEMENT	
1	1		R NR B	T S D			
2	1		R NR B	T S D			
3	1		R NR B	T S D			
4	1		R NR B	T S D			
5	1		R NR B	T S D			
6	1		R NR B	T S D			
7	1		R NR B	T S D			
8	1		R NR B	T S D			
9	1		R NR B	T S D			
10	1		R NR B	T S D			

TECHNOLOGY DATA BASE IDENTIFIER

[illegible]

HYPOTHETICAL TECH DE

MEMORY DEVICE DEFINITION

IDENTIFIER: 32-AEM-109

TYPE:

ACOM

RAMM

RRAM

MS

534

[illegible]

TECHNOLOGY DATA BASE IDENTIFIER HYPERLINK FILE

DEVICE IDENTIFIER	BASIC TRANSFER TO MAX UNITS MAX RATE (UNIT/SEC)	COMMUNICATION LINK DEVICE			
		TECH TYPE	DEVICE IDENTIFIER	TRANSMIT UNIT	RECEIVE RATE
HSD	3.2 B	04	0000000000000000	04	0000000000000000
	165.5	04	0000000000000000	04	0000000000000000
	165.5	04	0000000000000000	04	0000000000000000
BUS	3.2 B.15	04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000
		04	0000000000000000	04	0000000000000000

PAGE 13 OF 14

BASELINE SOFTWARE APPLICATION IDENTIFICATION

DATA BLOCK DEFINITIONS

ID	LEVEL	DISCIPLINE	SYSTEM INTERFACE DEVICE	MAXIMUM RECORDS	MINIMUM BITS/ BYTE WORD	RECORD SIZE IN WORDS		
						MINIMUM	AVERAGE	MAXIMUM
PANL	5	PANL	MM-113	128	4			
PLANLITE	5	PANL	MM-113	256	4			
CAOMAT	5	CBME	CL-113SD	2	4	128	128	128
DOREAH	5	PANL	CL-113SD	100	4			
MODPLIST	5	PANL	CL-113SD	20	4			
CAIPL	5	CBME	CL-113SD	2	4	128	128	128
DYNADATA	5	PANL	CL-113SD	8192	4			
SIMPOS	5	CBME	CL-113SD-4	2	4	128	128	128
SWIPPOS	5	CBME	MM-111	2	4	128	128	128
CL	5	PANL		1024	4			
ADOTD	5	PANL		512	4			
POTIC	5	PANL		512	4			
COMETATA	5	PANL		512	4			
DYNADATASW	5	PANL	MM-113		4			
	5				4			

SAMPLE APPLICATION

DATE 11-3-41
BY STA AG 111100 (10)

ENABLEMENT TYPE: TIME
L AILEU ADEL: ADEL ADEL

DATA Q / MASTER TASK;
(11 1/2) 111 SLAVED)

MAXIMUM TIME: _____
FREQUENCY: _____ 30

INSTRUCTION MIX				TASK I/O PER EXECUTION			
INSTRUCTION NO.	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT	START* ALONG END	RECORDS PROCESSED MIN AVE MAX
1	1000000	1000000	1000000	SYMPAS	010	01E	1000000
2	1000000	1000000	1000000	SYMPAS	010	01E	1000000
3	1000000	1000000	1000000	SYMPAS	010	01E	1000000
4	1000000	1000000	1000000	SYMPAS	010	01E	1000000
5	1000000	1000000	1000000	SYMPAS	010	01E	1000000
6	1000000	1000000	1000000	SYMPAS	010	01E	1000000
7	1000000	1000000	1000000	SYMPAS	010	01E	1000000
8	1000000	1000000	1000000	SYMPAS	010	01E	1000000
9	1000000	1000000	1000000	SYMPAS	010	01E	1000000
10	1000000	1000000	1000000	SYMPAS	010	01E	1000000
11	1000000	1000000	1000000	SYMPAS	010	01E	1000000
12	1000000	1000000	1000000	SYMPAS	010	01E	1000000
13	1000000	1000000	1000000	SYMPAS	010	01E	1000000
14	1000000	1000000	1000000	SYMPAS	010	01E	1000000
15	1000000	1000000	1000000	SYMPAS	010	01E	1000000
16	1000000	1000000	1000000	SYMPAS	010	01E	1000000
17	1000000	1000000	1000000	SYMPAS	010	01E	1000000
18	1000000	1000000	1000000	SYMPAS	010	01E	1000000
19	1000000	1000000	1000000	SYMPAS	010	01E	1000000
20	1000000	1000000	1000000	SYMPAS	010	01E	1000000
21	1000000	1000000	1000000	SYMPAS	010	01E	1000000
22	1000000	1000000	1000000	SYMPAS	010	01E	1000000
23	1000000	1000000	1000000	SYMPAS	010	01E	1000000
24	1000000	1000000	1000000	SYMPAS	010	01E	1000000
25	1000000	1000000	1000000	SYMPAS	010	01E	1000000
26	1000000	1000000	1000000	SYMPAS	010	01E	1000000
27	1000000	1000000	1000000	SYMPAS	010	01E	1000000
28	1000000	1000000	1000000	SYMPAS	010	01E	1000000
29	1000000	1000000	1000000	SYMPAS	010	01E	1000000
30	1000000	1000000	1000000	SYMPAS	010	01E	1000000
31	1000000	1000000	1000000	SYMPAS	010	01E	1000000
32	1000000	1000000	1000000	SYMPAS	010	01E	1000000
33	1000000	1000000	1000000	SYMPAS	010	01E	1000000
34	1000000	1000000	1000000	SYMPAS	010	01E	1000000
35	1000000	1000000	1000000	SYMPAS	010	01E	1000000
36	1000000	1000000	1000000	SYMPAS	010	01E	1000000
37	1000000	1000000	1000000	SYMPAS	010	01E	1000000
38	1000000	1000000	1000000	SYMPAS	010	01E	1000000
39	1000000	1000000	1000000	SYMPAS	010	01E	1000000
40	1000000	1000000	1000000	SYMPAS	010	01E	1000000
41	1000000	1000000	1000000	SYMPAS	010	01E	1000000
42	1000000	1000000	1000000	SYMPAS	010	01E	1000000
43	1000000	1000000	1000000	SYMPAS	010	01E	1000000
44	1000000	1000000	1000000	SYMPAS	010	01E	1000000
45	1000000	1000000	1000000	SYMPAS	010	01E	1000000
46	1000000	1000000	1000000	SYMPAS	010	01E	1000000
47	1000000	1000000	1000000	SYMPAS	010	01E	1000000
48	1000000	1000000	1000000	SYMPAS	010	01E	1000000
49	1000000	1000000	1000000	SYMPAS	010	01E	1000000
50	1000000	1000000	1000000	SYMPAS	010	01E	1000000
51	1000000	1000000	1000000	SYMPAS	010	01E	1000000
52	1000000	1000000	1000000	SYMPAS	010	01E	1000000
53	1000000	1000000	1000000	SYMPAS	010	01E	1000000
54	1000000	1000000	1000000	SYMPAS	010	01E	1000000
55	1000000	1000000	1000000	SYMPAS	010	01E	1000000
56	1000000	1000000	1000000	SYMPAS	010	01E	1000000
57	1000000	1000000	1000000	SYMPAS	010	01E	1000000
58	1000000	1000000	1000000	SYMPAS	010	01E	1000000
59	1000000	1000000	1000000	SYMPAS	010	01E	1000000
60	1000000	1000000	1000000	SYMPAS	010	01E	1000000
61	1000000	1000000	1000000	SYMPAS	010	01E	1000000
62	1000000	1000000	1000000	SYMPAS	010	01E	1000000
63	1000000	1000000	1000000	SYMPAS	010	01E	1000000
64	1000000	1000000	1000000	SYMPAS	010	01E	1000000
65	1000000	1000000	1000000	SYMPAS	010	01E	1000000
66	1000000	1000000	1000000	SYMPAS	010	01E	1000000
67	1000000	1000000	1000000	SYMPAS	010	01E	1000000
68	1000000	1000000	1000000	SYMPAS	010	01E	1000000
69	1000000	1000000	1000000	SYMPAS	010	01E	1000000
70	1000000	1000000	1000000	SYMPAS	010	01E	1000000
71	1000000	1000000	1000000	SYMPAS	010	01E	1000000
72	1000000	1000000	1000000	SYMPAS	010	01E	1000000
73	1000000	1000000	1000000	SYMPAS	010	01E	1000000
74	1000000	1000000	1000000	SYMPAS	010	01E	1000000
75	1000000	1000000	1000000	SYMPAS	010	01E	1000000
76	1000000	1000000	1000000	SYMPAS	010	01E	1000000
77	1000000	1000000	1000000	SYMPAS	010	01E	1000000
78	1000000	1000000	1000000	SYMPAS	010	01E	1000000
79	1000000	1000000	1000000	SYMPAS	010	01E	1000000
80	1000000	1000000	1000000	SYMPAS	010	01E	1000000
81	1000000	1000000	1000000	SYMPAS	010	01E	1000000
82	1000000	1000000	1000000	SYMPAS	010	01E	1000000
83	1000000	1000000	1000000	SYMPAS	010	01E	1000000
84	1000000	1000000	1000000	SYMPAS	010	01E	1000000
85	1000000	1000000	1000000	SYMPAS	010	01E	1000000
86	1000000	1000000	1000000	SYMPAS	010	01E	1000000
87	1000000	1000000	1000000	SYMPAS	010	01E	1000000
88	1000000	1000000	1000000	SYMPAS	010	01E	1000000
89	1000000	1000000	1000000	SYMPAS	010	01E	1000000
90	1000000	1000000	1000000	SYMPAS	010	01E	1000000
91	1000000	1000000	1000000	SYMPAS	010	01E	1000000
92	1000000	1000000	1000000	SYMPAS	010	01E	1000000
93	1000000	1000000	1000000	SYMPAS	010	01E	1000000
94	1000000	1000000	1000000	SYMPAS	010	01E	1000000
95	1000000	1000000	1000000	SYMPAS	010	01E	1000000
96	1000000	1000000	1000000	SYMPAS	010	01E	1000000
97	1000000	1000000	1000000	SYMPAS	010	01E	1000000
98	1000000	1000000	1000000	SYMPAS	010	01E	1000000
99	1000000	1000000	1000000	SYMPAS	010	01E	1000000
100	1000000	1000000	1000000	SYMPAS	010	01E	1000000

CIRCLE ONE PER ENTRY

BASISLINE SOFTWARE APPLICATION IDENTIFICATION

TASK: 711-6 TASK DEFINITION: 711-3

ENABLEMENT TYPE: SL-V3 MASTER TASK: (IF SLAVED) 711-3

LANGUAGE: FORTRAN IV FREQUENCY: 300

OVERLAY: YES (NO)

MAXIMUM TIME: 300

INSTRUCTION MIX			TASK I/O PER EXECUTION			
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	INPUT* UPDATE ALONG OUTPUT	START* ALONG END	RECORDS PROCESSED MIN AVE MAX
1	1000000	1000000	1000000	100	100	100 20 40
2	1000000	1000000	1000000	100	100	100 20 40
3	1000000	1000000	1000000	100	100	100 20 40
4	1000000	1000000	1000000	100	100	100 20 40
5	1000000	1000000	1000000	100	100	100 20 40
6	1000000	1000000	1000000	100	100	100 20 40
7	1000000	1000000	1000000	100	100	100 20 40
8	1000000	1000000	1000000	100	100	100 20 40
9	1000000	1000000	1000000	100	100	100 20 40
10	1000000	1000000	1000000	100	100	100 20 40
11	1000000	1000000	1000000	100	100	100 20 40
12	1000000	1000000	1000000	100	100	100 20 40
13	1000000	1000000	1000000	100	100	100 20 40
14	1000000	1000000	1000000	100	100	100 20 40
15	1000000	1000000	1000000	100	100	100 20 40
16	1000000	1000000	1000000	100	100	100 20 40
17	1000000	1000000	1000000	100	100	100 20 40
18	1000000	1000000	1000000	100	100	100 20 40
19	1000000	1000000	1000000	100	100	100 20 40
20	1000000	1000000	1000000	100	100	100 20 40
21	1000000	1000000	1000000	100	100	100 20 40
22	1000000	1000000	1000000	100	100	100 20 40
23	1000000	1000000	1000000	100	100	100 20 40
24	1000000	1000000	1000000	100	100	100 20 40
25	1000000	1000000	1000000	100	100	100 20 40
26	1000000	1000000	1000000	100	100	100 20 40
27	1000000	1000000	1000000	100	100	100 20 40
28	1000000	1000000	1000000	100	100	100 20 40
29	1000000	1000000	1000000	100	100	100 20 40
30	1000000	1000000	1000000	100	100	100 20 40
31	1000000	1000000	1000000	100	100	100 20 40
32	1000000	1000000	1000000	100	100	100 20 40
33	1000000	1000000	1000000	100	100	100 20 40
34	1000000	1000000	1000000	100	100	100 20 40
35	1000000	1000000	1000000	100	100	100 20 40
36	1000000	1000000	1000000	100	100	100 20 40
37	1000000	1000000	1000000	100	100	100 20 40
38	1000000	1000000	1000000	100	100	100 20 40
39	1000000	1000000	1000000	100	100	100 20 40
40	1000000	1000000	1000000	100	100	100 20 40
41	1000000	1000000	1000000	100	100	100 20 40
42	1000000	1000000	1000000	100	100	100 20 40
43	1000000	1000000	1000000	100	100	100 20 40
44	1000000	1000000	1000000	100	100	100 20 40
45	1000000	1000000	1000000	100	100	100 20 40
46	1000000	1000000	1000000	100	100	100 20 40
47	1000000	1000000	1000000	100	100	100 20 40
48	1000000	1000000	1000000	100	100	100 20 40
49	1000000	1000000	1000000	100	100	100 20 40
50	1000000	1000000	1000000	100	100	100 20 40
51	1000000	1000000	1000000	100	100	100 2

* CIRCLE ONE PER ENTRY

SAMPLE APPLICATION

MAXIMUM TIME: 11:11
FREQUENCY: 27

[illegible]

*** CIRCLE ONE PER ENTRY**

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BASIS LINE SOFTWARE APPLICATION IDENTIFICATION **SAMPLE APPLICATION**

TASK **37-13** TASK DEFINITION MASTER TASK: **10-1** MAXIMUM TIME: **100**
 OVERLAY: YES **(NO)** ENABLEMENT TYPE: **SLAVE** FREQUENCY: **100**
 LANGUAGE: **FORTRAN**

INSTRUCTION MIX				TASK I/O PER EXECUTION			
INSTRUCTION ID	SIZING COUNT	AVERAGE EXECUTIONS	MAXIMUM EXECUTIONS	DATA BLOCK	INPUT* UPDATE OUTPUT END	START* STOP LONG END	RECORDS PROCESSED MIN AVE MAX
100	100	100	100	DATA	100	100	100
101	100	100	100	DATA	100	100	100
102	100	100	100	DATA	100	100	100
103	100	100	100	DATA	100	100	100
104	100	100	100	DATA	100	100	100
105	100	100	100	DATA	100	100	100
106	100	100	100	DATA	100	100	100
107	100	100	100	DATA	100	100	100
108	100	100	100	DATA	100	100	100
109	100	100	100	DATA	100	100	100
110	100	100	100	DATA	100	100	100
111	100	100	100	DATA	100	100	100
112	100	100	100	DATA	100	100	100
113	100	100	100	DATA	100	100	100
114	100	100	100	DATA	100	100	100
115	100	100	100	DATA	100	100	100
116	100	100	100	DATA	100	100	100
117	100	100	100	DATA	100	100	100
118	100	100	100	DATA	100	100	100
119	100	100	100	DATA	100	100	100
120	100	100	100	DATA	100	100	100
121	100	100	100	DATA	100	100	100
122	100	100	100	DATA	100	100	100
123	100	100	100	DATA	100	100	100
124	100	100	100	DATA	100	100	100
125	100	100	100	DATA	100	100	100
126	100	100	100	DATA	100	100	100
127	100	100	100	DATA	100	100	100
128	100	100	100	DATA	100	100	100
129	100	100	100	DATA	100	100	100
130	100	100	100	DATA	100	100	100
131	100	100	100	DATA	100	100	100
132	100	100	100	DATA	100	100	100
133	100	100	100	DATA	100	100	100
134	100	100	100	DATA	100	100	100
135	100	100	100	DATA	100	100	100
136	100	100	100	DATA	100	100	100
137	100	100	100	DATA	100	100	100
138	100	100	100	DATA	100	100	100
139	100	100	100	DATA	100	100	100
140	100	100	100	DATA	100	100	100
141	100	100	100	DATA	100	100	100
142	100	100	100	DATA	100	100	100
143	100	100	100	DATA	100	100	100
144	100	100	100	DATA	100	100	100
145	100	100	100	DATA	100	100	100
146	100	100	100	DATA	100	100	100
147	100	100	100	DATA	100	100	100
148	100	100	100	DATA	100	100	100
149	100	100	100	DATA	100	100	100
150	100	100	100	DATA	100	100	100
151	100	100	100	DATA	100	100	100
152	100	100	100	DATA	100	100	100
153	100	100	100	DATA	100	100	100
154	100	100	100	DATA	100	100	100
155	100	100	100	DATA	100	100	100
156	100	100	100	DATA	100	100	100
157	100	100	100	DATA	100	100	100
158	100	100	100	DATA	100	100	100
159	100	100	100	DATA	100	100	100
160	100	100	100	DATA	100	100	100
161	100	100	100	DATA	100	100	100
162	100	100	100	DATA	100	100	100
163	100	100	100	DATA	100	100	100
164	100	100	100	DATA	100	100	100
165	100	100	100	DATA	100	100	100
166	100	100	100	DATA	100	100	100
167	100	100	100	DATA	100	100	100
168	100	100	100	DATA	100	100	100
169	100	100	100	DATA	100	100	100
170	100	100	100	DATA	100	100	100
171	100	100	100	DATA	100	100	100
172	100	100	100	DATA	100	100	100
173	100	100	100	DATA	100	100	100
174	100	100	100	DATA	100	100	100
175	100	100	100	DATA	100	100	100
176	100	100	100	DATA	100	100	100
177	100	100	100	DATA	100	100	100
178	100	100	100	DATA	100	100	100
179	100	100	100	DATA	100	100	100
180	100	100	100	DATA	100	100	100
181	100	100	100	DATA	100	100	100
182	100	100	100	DATA	100	100	100
183	100	100	100	DATA	100	100	100
184	100	100	100	DATA	100	100	100
185	100	100	100	DATA	100	100	100
186	100	100	100	DATA	100	100	100
187	100	100	100	DATA	100	100	100
188	100	100	100	DATA	100	100	100
189	100	100	100	DATA	100	100	100
190	100	100	100	DATA	100	100	100
191	100	100	100	DATA	100	100	100
192	100	100	100	DATA	100	100	100
193	100	100	100	DATA	100	100	100
194	100	100	100	DATA	100	100	100
195	100	100	100	DATA	100	100	100
196	100	100	100	DATA	100	100	100
197	100	100	100	DATA	100	100	100
198	100	100	100	DATA	100	100	100
199	100	100	100	DATA	100	100	100

* CIRCLE ONE PER ENTRY

**MASTER TASK:
(IF SLAVED)**

MAXIMUM TIME: _____

FREQUENCY: _____

• CIRCLE ONE PER ENTRY

ONLINE SOFTWARE APPLICATION IDENTIFICATION

TASK	TASK DEFINITION	ENABLEMENT TYPE:	MASTER TASK: (IF SLAVED)	MAXIMUM TIME:	FREQUENCY:
1148113		SLAV	114-1		
UNRELAY: YES (NO)		LANGUAGE: FORTY-AN IV			

[illegible]

• CIRCLE ONE PER ENTRY

EVALUATION RUN IDENTIFICATION GLOBAL PARTITION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT IDENTIFIER	VALUE IF APP.
F	D	PARA	M3	
F	D	DR.LITE	M3	
F	D	CARDUT	M4	
F	D	AD.B.H	M3	
F	D	MOD.P.LIST	M3	
F	D	CAL.PT	M4	
F	D	DY.ND.ATA	M3	
F	D	EMPOS	M1	
F	D	RAWPOS	M1	

EVALUATION RUN IDENTIFICATION GLOBAL CONFIGURATION EX

PARTITIONING ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE F - FIXED I - INITIAL P - PROHIBITED	COMPONENT ASSIGNMENT D - DATA T - TASK	APPLICATION COMPONENT IDENTIFIER	CANDIDATE CONFIGURATION COMPONENT IDENTIFIER VALUE IF APP.
F	D	GL	M3
I	D	ADATAI	M1
I	D	BDATAI	M2
I	D	BDMDATAI	M3
F	D	DYNDAI,ASW	M3

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETICAL TECH DB

INSTRUCTION BENCHMARK <u>BA2</u>		ON PROCESSOR <u>HYPER/75</u> USING <u>HYPER/75</u> OPERATING SYSTEM	
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) FETCHES	DEVELOPMENT (MAN-YEARS) ONE TIME PER OCCURRENCE
AVERAGE	<u>1000</u>	<u>111111</u>	<u>111111</u>
WORST CASE	<u>111111</u>	<u>111111</u>	<u>111111</u>
LANGUAGE FACTORS:			
1 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
2 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
3 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
4 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
5 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
6 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
7 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>
8 <u>111111</u>	<u>111111</u>	<u>111111</u>	<u>111111</u>

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK <u>ELR</u>		ON PROCESSOR <u>486/25</u>		USING <u>286-25</u> OPERATING SYSTEM	
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORIES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME PER OCCURRENCE
AVERAGE	<u>100</u>				
WORST CASE					
LANGUAGE FACTORS:					
1					
2					
3					
4					
5					
6					
7					
8					

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETALLIC TECH DB

INSTRUCTION BENCHMARK <u>CMR85TIRAI.MP</u>		ON PROCESSOR <u>8X2321/75</u> USING <u>OS-5V2-3P</u> OPERATING SYSTEM				
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURRENCE
AVERAGE	<u>809</u>	<u>31</u>	<u>140</u>	<u>70</u>		
WORST CASE						
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK <u>BMPI</u>		ON PROCESSOR <u>XYZ32175</u> USING <u>OS-XYZ-23</u> OPERATING SYSTEM				
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURRENCE
AVERAGE	<u>3999</u>					
WORST CASE						
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETICAL II, CA, 198

INSTRUCTION BENCHMARK <u>CARCASMAT</u>				ON PROCESSOR <u>XY232/75</u> USING <u>OS-XY2-23</u> OPERATING SYSTEM			
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURRENCE	
AVERAGE	<u>3,000</u>			<u>2222</u>			
WORST CASE				<u>2222</u>			
LANGUAGE FACTORS:							
1							
2							
3							
4							
5							
6							
7							
8							

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK <u>CONFIDENTIAL</u>					ON PROCESSOR <u>8X232/75</u> USING <u>Q5-8X7-23</u> OPERATING SYSTEM	
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	<u>4800</u>			<u>4444</u>	<u>0</u>	<u>00000000</u>
WORST CASE				<u>4444</u>		<u>00000050</u>
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETRIC TECH DB

INSTRUCTION BENCHMARK <u>PRJITAD</u>		ON PROCESSOR <u>XYZ32/75</u>		USING <u>OS-XN-26</u> OPERATING SYSTEM	
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME PER OCCURRENCE
AVERAGE	<u>800</u>	<u> </u>	<u> </u>	<u>556</u>	<u>5</u> <u>16</u>
WORST CASE	<u> </u>	<u> </u>	<u> </u>	<u>556</u>	<u> </u> <u>25</u>
LANGUAGE FACTORS:					
1 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
2 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
3 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
4 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
5 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
6 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
7 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
8 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>

TECHNOLOGY DATA BASE IDENTIFIER

INSTRUCTION BENCHMARK		ON PROCESSOR				OPERATING SYSTEM	
INSTRUCTION BENCHMARK		ON PROCESSOR				OPERATING SYSTEM	
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INSTRUCTION BENCHMARK		ON PROCESSOR				OPERATING SYSTEM	

HYPOTHETICAL TECH. DB

BASIC MEASUREMENTS	INSTRUCTION BENCHMARK <u>HOARDMAN</u>	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	OPERATING SYSTEM	
						DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURRENCE
AVERAGE		<u>1200</u>	<u>208</u>	<u>208</u>	<u>416</u>	<u>26</u>	<u>26</u>
WORST CASE							
LANGUAGE FACTORS:							
1 <u>FORTRAN IV</u>		<u>1</u>	<u>208</u>	<u>208</u>	<u>416</u>	<u>26</u>	<u>26</u>
2 <u>ASSIMBLER</u>		<u>208</u>	<u>208</u>	<u>208</u>	<u>208</u>	<u>416</u>	<u>26</u>
3							
4							
5							
6							
7							
8							

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECHNOLOGY

INSTRUCTION BENCHMARK			ON PROCESSOR <u>XYZ22/75</u> USING <u>DS-V-VI-2</u> OPERATING SYSTEM			
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURANCE
AVERAGE	<u>800</u>			<u>555</u>		
WORST CASE				<u>555</u>		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH.D3

INSTRUCTION BENCHMARK <u>WISDOM</u>		ON PROCESSOR <u>8Y32/75</u> USING <u>DS-X-12-28</u> OPERATING SYSTEM				
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME	PER OCCURRENCE
AVERAGE	<u>800</u>			<u>555</u>		
WORST CASE				<u>555</u>		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETRIC TECH 03

INSTRUCTION BENCHMARK <u>EDYM</u>		ON PROCESSOR <u>XY232/75</u> USING <u>OS-X-72-23</u> OPERATING SYSTEM				
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURRENCE
AVERAGE	<u>100</u>			<u>555</u>		
WORST CASE				<u>555</u>		
LANGUAGE FACTORS:						
1						
2						
3						
4						
5						
6						
7						
8						

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK <u>PEV</u>		ON PROCESSOR <u>XYZ-2R</u> OPERATING SYSTEM USING <u>Q5-XYZ-2R</u>	
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	TIMING (CYCLES) FETCHES	DEVELOPMENT (MAN YEARS) ONE TIME PER OCCURRENCE
AVERAGE	<u>129</u>		
WORST CASE			
LANGUAGE FACTORS:			
1			
2			
3			
4			
5			
6			
7			
8			

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH 705

INSTRUCTION BENCHMARK <u>8000</u>				ON PROCESSOR <u>8000/75</u> USING <u>DS-8000-25</u> OPERATING SYSTEM	
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME PER OCCURRENCE
AVERAGE	<u>3000</u>	<u> </u>	<u> </u>	<u>2222</u>	<u> </u>
WORST CASE	<u> </u>	<u> </u>	<u> </u>	<u>2222</u>	<u> </u>
LANGUAGE FACTORS:					
1 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
2 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
3 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
4 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
5 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
6 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
7 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
8 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>

TECHNOLOGY DATA BASE IDENTIFIER HYPERMETRICAL TECH DB

INSTRUCTION BENCHMARK <u>80000</u>					
		ON PROCESSOR <u>XX232/75</u> USING <u>OS-X2-2B</u> OPERATING SYSTEM			
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME PER OCCURANCE
AVERAGE	<u>3000</u>			<u>2222</u>	
WORST CASE				<u>2222</u>	
LANGUAGE FACTORS:					
1					
2					
3					
4					
5					
6					
7					
8					

TECHNOLOGY DATA BASE IDENTIFIER HYPOTHETICAL TECH DB

INSTRUCTION BENCHMARK <u>SHIPALOT</u>			ON PROCESSOR <u>XXZ32/15</u> USING <u>Q5-X72-W33</u> OPERATING SYSTEM			
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN YEARS) ONE TIME	PER OCCURANCE
AVERAGE	<u>120</u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
WORST CASE	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
LANGUAGE FACTORS:						
1 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
2 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
3 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
4 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
5 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
6 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
7 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>
8 <u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>

ST. HILARY CATHOLIC SCHOOL

BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME PER OCCURRENCE
AVERAGE	1,000				
WORST CASE					
LANGUAGE FACTORS:					
1					
2					
3					
4					
5					
6					
7					
8					

TECHNOLOGY DATA BASE IDENTIFIER

INSTRUCTION BENCHMARK		ON PROCESSOR		OPERATING SYSTEM	
		USING			
BASIC MEASUREMENTS	SIZING (BYTES) USER CODE	STORES	TIMING (CYCLES) FETCHES	COMPUTATIONAL	DEVELOPMENT (MAN-YEARS) ONE TIME PER OCCURRENCE
AVERAGE	20				95
WONST CASE					
LANGUAGE FACTORS:					
1					
2					
3					
4					
5					
6					
7					
8					

C.3 INTERMEDIATE VALUES

PROCESSOR BALANCE CASE 1

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
AL 1a	TASK	UTIL	TASK	UTIL	TASK	UTIL	
	1	50	5	40	6	20	$J = 1, IJT = 4, IJLIST = 1, 3, 4, 2$ $K = 3$
	2	10					
	3	25					
	4	15					
	$U_1 = 100$		$U_2 = 40$		$U_3 = 20$		Set Limit PTOL 1. Amount to offload to meet limit $U_j - L_j = 100 - 75 = 25$
							2. Amount which K can take on $G_K - U_K = 60 - 20 = 40$
							3. Heuristic decision is to take minimum of {J offload amount, K's amount to goal} $= \text{minimum } \{25, 40\} = 25$
	1	50	5	40	6	30	Therefore, PTOL = 25
	2	10					Process candidate task list
	4	15			3	25	1. Find task utilization closest to PTOL. In this case, Task 3 is selected. Verify Task 3 can be performed on processor K = 3; i.e., all real-time constraints are met.
	$U_1 = 75$		$U_2 = 40$		$U_3 = 45$		2. Make full allocation if such a task exists.
	Note at this point U_1 meets absolute limit branch to general balance algorithm.						

AL - above limit heuristic
ISSUE

GB - general balance heuristic
DATE

ID LOADBL

SEC CASE 1

PAGE 1/4

PROCESSOR BALANCE CASE 1 CONTINUED

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
	TASK	UTIL	TASK	UTIL	TASK	UTIL	
GB 1a	1	50	5	40	6	20	$1J = NP - MPGL = 3 - 0 = 3$ $IK = 1, ITER = 0$ $CDPCOI = 3, 2, 1$ (ranking with respect to goal deviation in descending order)
	2	10			3	25	
	4	15					
	$U_1 = 75$ $U_1 = -15$		$U_2 = 40$ $U_2 = 0$		$U_3 = 45$ $U_3 = +15$		
							<p>Compute highest and lowest processor indices</p> $IHI = CDPCOI(1J) = 1$ $ILD = CDPCOI(1K) = 3$ <p>Compute GPUSOL</p> $= U_{ILD} - U_{IHI} = U_3 - U_1 = 15 - (-15) = 30$ <p>Perform convergence test</p> $GPUSOL \leq GTOLPU$ $\Rightarrow 30 \leq 5$ <p>False continue to iterate</p> $ITER = ITER + 1 = 1$ <p>Maximum iteration</p> $ITER \leq MPITER$ $1 \leq 10$ <p>False implies perform balance loop</p>

PROCESSOR BALANCE CASE 1 CONTINUED

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
TASK	TASK	UTIL	TASK	UTIL	TASK	UTIL	
G8 1a Cont	1	50	5	40	6	20	<p>$L = 3$ $J = \text{CDPCDI } (L) = 1$ processor to be offloaded</p> <p>Candidate task list $IJT = 3, IJLIST = 1, 4, 2$</p> <p>Set limit to offload = PTOL</p> <p>1. Amount to balance between processors J and K $= \frac{U_K^1 - U_J^1}{2} = \frac{15 - (-15)}{2} = \frac{30}{2} = 15$</p> <p>2. Amount K and take on and not exceed goal $= G_K - U_K = G_3 - U_3^1 = 60 - 45 = 15$</p> <p>3. Minimum (balance value, limit value) = 15</p> <p>Process candidate task list for task closest to 15% utilization on processor J -- in this case, task 4</p>
	2	10			3	25	
	4	15					
	U_1	= 75	U_2	= 40	U_3	= 45	
	U_1^1	= -15	U_2^1	= 0	U_3^1	= +15	

PROCESSOR BALANCE CASE 1 CONCLUDED

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
68 la con't	TASK	UTIL	TASK	UTIL	TASK	UTIL	<p>Confirm task 4 can meet all real-time constraints if allocated to processor 3. If so make allocation.</p> <p>This is the case for this example as processors are identical and have one shared memory with no fixed or prohibited allocation of task 4.</p> <p>All processors at goal GPUSOL = 0 RETURN</p>
	1	50	5	40	6	20	
	2	10			3	25	
	4	15					
	U ₁	= 75	U ₂	= 40	U ₃	= 45	
	U ₁	= -15	U ₂	= 0	U ₃	= +15	
	1	50	5	40	6	20	
	2	10			3	25	
	U ₁	= 60	U ₂	= 40	U ₃	= 60	
	U ₁	= 0	U ₂	= 0	U ₃	= 0	

PROCESSOR BALANCE CASE 2

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
	TASK	UTIL	TASK	UTIL	TASK	UTIL	
AL 1	1	50	5	40	6	20	Same as Case 1 Except instruction block for task 3 must be moved to private memory for processor 3
	2	10					
	3	25					
	4	15					
GB 1a	1	50	5	40	6	20	Same as Case 1 Except instruction block for task 4 must be moved to private memory for processor 3
	2	10			3	25	
	4	15					

PROCESSOR BALANCE CASE 3

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
AL 1a	TASK	UTIL	TASK	UTIL	TASK	UTIL	<p>Same as Case 1 Except tasks 1 and 3 cannot be allocated to processor 3 and alternate task allocation is sought which is close to 25% (PTOL for AL1)</p> <p>IJLIST = 4, 2 IJT = 2</p> <p>Task 4 is selected and meets all real-time constraints and its instructions are moved to processor 3's private memory</p> <p>Note PR1 is still above limit. Continue task search for another potential task offload</p>
	X1	50	5	40	6	20	
	2	10					
	X3	25					
	4	15					
	U ₁ = 100		U ₂ = 20		U ₃ = 20		
	1	50					
	2	10					
	3	25					
	U ₁ = 85		U ₂ = 40		U ₃ = 35		

PROCESSOR BALANCE CASE 3 CONTINUED

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
A1b	TASK	UTIL	TASK	UTIL	TASK	UTIL	
	#1	50	5	40	6	20	Reset PTOL - the amount to be offloaded
	2	10			4	15	= $\min \{U_1 - L_1, U_3\}$
	#3	25					= $\min \{10, 25\}$
							= 10
	U_1	= 85	U_2	= 40	U_3	= 35	Search remaining candidate tasks for one closest to 10
	U_j	= -110	U_j	= 0	U_j	= 25	= Task 2
	#1	50	5	40	6	20	Confirm task 2 can be performed on Processor 3 by moving instructions to private memory for processor 3
	#3	25			4	15	Make allocation of task 2 to processor 3
	U_1	= 75	U_2	= 40	2	10	
	U_j	= -15	U_j	= 0	U_3	= 45	
					U_j	= +15	
	Note processor 1 is now at limit value. Go to balance loop.						

PROCESSOR BALANCE CASE 3 CONTINUED

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
	TASK	UTIL	TASK	UTIL	TASK	UTIL	
681	1	50	5	40	6	20	Ranks processor wrt goal utilization in descending order
	3	25			4	15	
					2	10	
	$U_1 =$	75	$U_2 =$	40	$U_3 =$	45	CDPCDI = 3, 2, 1
	$U_j =$	-15	$U_j =$	0	$U_j =$	+15	MPGTL = MPGTL = 0
							None of the processors are above their limit
							ITER = 0
							IJ = MP - MPGTL = 3 - 0 = 3
							IK = 1
							Retrieve index to current high and low utilized processors
							IHI = CDPCDI (IJ) = CDPCDI (3) = 1
							ILO = CDPCDI (IK) = CDPCDI (1) = 3
							Check balance between high and low
							GPUSOL = CDPCD (ILO) - CDPCD (IHI) = +15 - (-15) = 30
							Compare with balance tolerance
							GPUSOL \leq 5
							False continue to iterate
							ITER = ITER + 1 = 0 + 1 = 1

PROCESSOR BALANCE CASE 3 CONCLUDED

ITERATION	PR1		PR2		PR3		INTERMEDIATE CALCULATIONS
GB1	TASK	UTIL	TASK	UTIL	TASK	UTIL	Maximum iteration test
	#1	50	5	40	6	20	ITER .GT. 10
	#3	25			4	15	
					2	10	
	$U_1 = 75$ $U_1 = -15$		$U_2 = 40$ $U_2 = 0$		$U_3 = 45$ $U_3 = +15$		No continue balance process K = 110 least loaded processor remaining in balance loop L = 1J = 3 index to overloaded processor index J = CDPCDI (L) = CDPCDI (3) = 1 CDPCD (K) .GT. CDPCD (J) CDPCD (3) .GT. CDPCD (J) True continue task offload process Build candidate task list to offload from processor j T3 fixed Leave Task 1 Task 1 cannot be placed on 3 Bottleneck condition is diagnosed

MEMORY BALANCE CASE 1

ITERATION	M1 BLOCK	M1 UTIL	M2 BLOCK	M2 UTIL	INTERMEDIATE CALCULATIONS
AL1	1 2 3 $U_1 = 80$	10 30 40	4 $U_2 = 20$	20	$U_1 - L_1 = 80 - 70 = 10$ amount to make limit $(U_1 - U_2)/2 = (80 - 20)/2 = 30$ amount to balance $G_2 - U_2 = (60 - 20) = 40$ maximum M2 can take on Minimum {10, 30, 40} = 10 Transfer block 1
GB1	2 3 $U_1 = 70$	30 40 70	4 1 $U_2 = 30$	20 10 30	All memories at or below limit switch to balance algorithm $\frac{1}{2} (U_1 - G_2) = (70 - 30)/2 = 20$ amount to balance $G_2 - U_2 = 60 - 30 = 30$ maximum M2 can take on Minimum {20, 30} = 20 block 2 block 3 block 2 Minimum {30 - 20, 40 - 20} = 30 Transfer block 2
GB2	3 $U_1 = 40$	40 40 10	4 1 2 $U_2 = 60$	20 10 30 60	$(U_2 - U_1)/2 = (60 - 40)/2 = 10$ amount to balance $G_1 - U_1 = 60 - 40 = 20$ maximum M1 can take on Minimum {10, 20} = 10 Select block 1 to go to M1 $U_2 - U_1 = 0$ implies "perfect" balance

AL - above limit iterations

GB - memory goal balance iterations

MEMORY BALANCE CASE 2

ITERATION	M1 BLOCK UTIL	M2 BLOCK UTIL	INTERMEDIATE CALCULATIONS
AL 1	<div>110</div> <div>230</div> <div>340</div> <div>U₁ = 80</div>	<div>420</div> <div>U₂ = 20</div>	Same as Case 1
GB 1	<div>230*</div> <div>340</div> <div>U₁ = 70</div>	<div>420</div> <div>110</div> <div>U₂ = 30</div>	$(U_1 - U_2)/2 = (70 - 30)/2 = 20$ balance amount $G_2 - U_2 = 60 - 30 = 30$ maximum to take on Minimum {20, 30} = 20 Note: Block 2 cannot be transferred Block 3 will cause M2 to exceed goal hence a bottleneck situation appears to be encountered.
AL 1 - SWAP	<div>230</div> <div>420</div> <div>U₁ = 50</div>	<div>340</div> <div>110</div> <div>U₂ = 50</div>	Swap check <div>2↔4-30 + 20-10-20 + 30+10</div> <div>*2↔1-30 + 10-20-10 + 30+20</div> <div>*3↔4-40 + 20-20-20 + 40+20</div> <div>3↔1-40 + 10-30-10 + 40+30</div> Alternate optimal swaps of 20 units added to M2

1/1

CASE 2

MEMBAL

MEMORY BALANCE CASE 3

ITERATION	M1 BLOCK UTIL	M2 BLOCK UTIL	INTERMEDIATE CALCULATIONS
AL1	<div> <div>1</div> <div>2</div> <div>3</div> <div>U₁ = 80</div> </div> <div> <div>10</div> <div>30</div> <div>40</div> </div>	<div> <div>4</div> <div>U₂ = 20</div> </div> <div> <div>20</div> </div>	<p> $U_1 - L_1 = 80 - 70 = 10$ amount to make limit $(U_1 - U_2)/2 = (80 - 20)/2 = 30$ amount to balance $G_2 - U_2 = (60 - 20) = 40$ maximum M2 can take on minimum {10, 30, 40} = 10 Transfer Block 1 </p>
GB1	<div> <div>2</div> <div>3</div> <div>U₁ = 70</div> </div> <div> <div>30</div> <div>40</div> </div>	<div> <div>4</div> <div>U₂ = 40</div> </div> <div> <div>20</div> <div>20</div> </div>	<p> $(U_1 - U_2)/2 = (70 - 40)/2 = 15$ $(G_2 - U_2) = (60 - 40) = 20$ Minimum {15, 20} Without swap neither block can be moved With swap trades </p>
GB1 - SWAP	<div> <div>1</div> <div>3</div> <div>U₁ = 50</div> </div> <div> <div>10</div> <div>40</div> <div>50</div> </div>	<div> <div>4</div> <div>U₂ = 50</div> </div> <div> <div>20</div> <div>30</div> <div>50</div> </div>	<p> NET M1 NET M2 2 ↔ 4 -30 + 20 = -10 -20 + 30 = +10 +2 ↔ 1 -30 + 10 = -20 -20 + 30 = +10 3 ↔ 4 -40 + 20 = -20 -20 + 40 = +20 3 ↔ 1 -40 + 10 = -30 -20 + 40 = +20 </p>

1/1

CASE 3

MEBAL

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
A_{t1}	TARRF(t,i) of DEALS IPT-9 GRP-11	F10.5	<p>= fraction of information input for task t from block i</p> <p>= $\frac{TARR(t,i,k)}{BLNMR (TAIOB(t,i))} = \frac{\text{Records Read}}{\text{Maximum Records for Block i}}$</p> <p>Example:</p> <p>TASK: T1-3 BLOCK: DIRLITE RECORDS REFERENCED = 120 for average case MAXIMUM RECORDS = 256</p> <p>$TARRF(t,i) = \frac{120}{256} = 0.5$</p> <p>NOTE: It is permissible for values to exceed 1 when multiple references are made by a task.</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
$a_{\text{mpt}i}$	MP SOL (m,p,e,3)	Nonnegative integer	<p>= the number of times input block i of task t is input for task t on processor p from memory m</p> <p>This is a function of the current solution variables:</p> <p>TPMAP(t,p,i) of DEALS IPT9 GRP8 MPMAP(m,p,i) of DEALS IPT9 GRP9 MEMAP(m,b,i) of DEALS IPT9 GRP10</p> <p>where $b = \text{TAIOB}(t,i)$ of DEALS IPT9 GRP12</p> <p>Actual implementation should consider a subroutine which computes this value for active solution entries as needed for decision making. The computation is more complex if duplicate blocks.</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
α_{mp}		0,1	<p>= 1 if access from memory m to processor p exists, i.e., there is at least one access link q for m and p</p> <p>= 0 if otherwise</p> <p>This switch may be computed by testing α_{mp} as follows:</p> <p>If ($\alpha_{mp} > 0$)</p> <p>Then $\alpha_{mp} = 1$</p> <p>Else $\alpha_{mp} = 0$</p> <p>NOTE:</p> <p>α_{mp} is design variable MPMP(m,p,1) of DEALS IPT9 GRP9.</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
α_{mp}	MPMAP (m.p.l) of IPT9 GRP9	Real ≥ 0	= bits/sec transfer rate from memory m to processor p based on statistical composite of access links for p and m

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
B	NB of DEALS IPT9 GRP2	Positive Integer $1 \leq NB \leq MB$ where MB is maximum number of blocks as defined in DEALS IPT9 GRP1	<ul style="list-style-type: none"> number of distinct storage blocks to be allocated to memories <p>This variable is computed by PASS1 PPD-1310 ADDBLK. It includes all data and task instruction blocks.</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
B	MB of DEALS IPT9 GRP1	Positive Integer	= maximum number of input and/or output blocks per task Specific algorithm implementation should provide a fixed upper limit or a dynamic computed upper limit as a function of the other major sizing variables P, T, B, Q, M

PAGE 6

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
C_{tk}			<p>= portion of task t which must be completed before the next dependent task in thread k may be enabled</p>

ISSUE DATE ID SEC PAGE 7

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
c_{tp}	TPVAL(t,p,1) IPT9 GRP8	Real > 0	= time for task t execution on processor p in seconds maintained to an accuracy of nanoseconds
Formula in English			
$= \text{Cycle Time} + \sum \left[\begin{array}{l} \text{Benchmark} \\ \text{Instruction} \\ \text{mix (computational +} \\ \text{fetch wait +} \\ \text{store wait)} \\ \text{cycles} \end{array} \right] + \text{Time Enablement Overhead} + \text{Data Enablement Overhead} + \text{Slaved Enablement Overhead} + \text{Overlay Overhead}$			
Example from Sample Problem 2 Tasks T14 and 16 on Processor A1			
$= 9 \times 10^{-7} + \left[1 * \underbrace{\left(\text{Comp } 416 + \text{Fetch } 208 + \text{Store } 208 \right)}_{\text{HOODDYN}} + 2 * \underbrace{\left(\text{Comp } 70 + \text{Fetch } 31 + \text{Store } 140 \right)}_{\text{BMBSTRALMP}} \right] + 0 + 0 + 1 \times 10^{-6} + 0$			
= 0.0011836 sec			

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
D_t	TADCS (t)	Real ≥ 0	<p>= development cost for task t in manyears</p> $= \sum_{p=1}^P [d_{tp} x_{tp} + \delta_{tp} x_{tp} - d_{tp} y_{tp}]$ <p>one time development resource management development duplicate utilization</p> <p>This parameter is computed for the initial solution and recomputed for each change that is made by the heuristic tradeoffs.</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS																				
d_{tp}	TPVAL(t,p,4) of DEALS IPT9 GRP8	Real ≥ 0	<p>= the cost coefficient for developing task t to run on processor p (independent of allocation) in many years exclusive of duplicated charges and one-time charges</p> <p>d_{tp} may be calculated as needed as follows:</p> $TANIM(t) = \sum_{i=1} (TAIMX(t,i,j) * TPOC(p,i,2,\lambda))$ <p>where TANIM(t) of DEALS IPT9 GRP12 = number of benchmark instruction for task t TAIMX(t,i,j) of DEALS IPT9 GRP12 = number of specification instruction i references; j = 2 → average number, j = 3 → worstcase number TPOC(p,i,2,\lambda) of DEALS IPT9-5 = development cost per instruction reference in language \lambda on processor p I = TAIMX(t,i,1) of DEALS IPT9 GRP12 \lambda = TASC(t) of DEALS IPT9 GRP12</p>																				
<p>EXAMPLE:</p> <p>AVERAGE COST FOR TASK T1-3 ON PROCESSOR A1</p> <table border="1"> <thead> <tr> <th>i</th><th>BENCHMARK id</th><th>AVERAGE COUNT</th><th>PROCESSOR COST</th></tr> </thead> <tbody> <tr> <td>1</td><td>STMIF</td><td>1</td><td>0.2500</td></tr> <tr> <td>2</td><td>CONIF</td><td>0</td><td>0.0027</td></tr> <tr> <td>3</td><td>DRLITADJ</td><td>1</td><td>0.1600</td></tr> <tr> <td>4</td><td>T3</td><td>1</td><td>0.0500</td></tr> </tbody> </table> <p>Development Cost = 0.4600</p>				i	BENCHMARK id	AVERAGE COUNT	PROCESSOR COST	1	STMIF	1	0.2500	2	CONIF	0	0.0027	3	DRLITADJ	1	0.1600	4	T3	1	0.0500
i	BENCHMARK id	AVERAGE COUNT	PROCESSOR COST																				
1	STMIF	1	0.2500																				
2	CONIF	0	0.0027																				
3	DRLITADJ	1	0.1600																				
4	T3	1	0.0500																				

MATH SYMBOL	DESIGN MEMORIC	VALUE	DEFINITION AND RELATED PARAMETERS
D	GDCSOL of DEALS IPT9 GRP3	F10.2	= total partition development cost estimate in manyears $N_t = \sum_{t=1}^t D_t$

ISSUE DATE ID SEC PAGE 11

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
δ_{tp}			<p>= the cost coefficient for resource management of task t development on processor p.</p> <p>This is a function of the current partition solution and the established technology data base parameters for the processor and task enablement type.</p> <p>For example, a processor may currently limit the maximum number of tasks it can handle. If the solution tries to exceed this number, an additional development cost penalty must be added. This applies to enablement type disciplines as well. Those parameters related to development cost are in IOPT5 GRP3 as a function of processor and operating system.</p>

MATH SYMBOL	DESIGN PNEUMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
e_{tp}	TPMAP(t,p,1) of DEALS IPT9 GRP12	Integer .GE.0 .LE.TAFRQ(t) of DEALS IPT9 GRP12	= the number of task t executions on processor p for evaluation problem time period This is a major output of PASS2/PASS3.

ISSUE

DATE

IC

SEC

PAGE 13

MATH SYMBOL	DESIGN PNEUMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
F_k	BLTIN(k,*) of DEALS IPT9 GRP13	Positive integers	<p>= a task thread defined as a group of serially dependent tasks with the following notation:</p> $F_k = \{f_{k1}, \dots, f_{kg_k}\}$ <p>where</p> $f_{kg} \equiv \text{BLTIN}(k, g) \text{ of IPT9 GRP13 thread } k \text{ task } g\text{'s}$ <p>index for $g = 1$ to G_k</p> $G_k \equiv \text{BLTNT}(k) \text{ of IPT9 GRP13 is the number of tasks in thread } k$

MATH SYMBOL	DESIGN MNEEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
G_p	CDPBU(p) of DEALS IPT9 GRP4	Positive real 0 .LT. G_p .LE. 1.00	= goal utilization for processor p

PAGE 15

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
q_m	CDMSU(m)	Positive real 0 .LT. q_m .LE. 1	= goal allocation for memory m

PAGE 16

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
h_b		Integer ≥ 1 \leq MH of IPT 9 GRP 1	<p>= number of memories where block b is stored</p> $h_b = \sum_{m=1}^{MH} MBMAP(m, b, 1)$ <p>MBMAP is probably best handled as a linked list (for each block) of active allocation due to anticipated sparse density.</p> <p>MBMAP of IPT9 GRP10</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
I_t		Nonnegative integer	<p>= number of distinct input blocks for task t</p> $TANIO(t) = \sum_{i=1} f(TAHBR(t,i))$ <p>where</p> $f(TAHBR(t,i)) = \begin{cases} = 1 & \text{if } TAHBR(t,i) = 1 \\ = 1 & \text{if } TAHBR(t,i) = 3 \\ = 0 & \text{otherwise} \end{cases}$ <p>$TAHBR(t,i)$ and $TANIO(t)$ are in IPT9 GRP12.</p>

MATH SYMBOL	DESIGN ANEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
i_{ti}	TAI08(t,i) of IPT9 GRP12	Positive integer	= global data block index for task t input block i provided that TAI08(t,i) = 1 or 3 TAI08(t,i) of IPT9 GRP12

ISSUE

DATE

ID

SEC

PAGE 19

PATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
L_m	CDMSZ(m) of DEALS IPT9 GRPS	Real > 0	<p>= length of memory m in bits</p> <p>$CDMSZ(m) = TMAUP(m,u,2) * CDMSA(m)$</p> <p>where</p> <p>$u = CDMSU(m)$ of DEALS IPT9 GRPS</p> <p>= index to unit of measure for memory m's sizing</p> <p>$TMAUP(m,u,2)$ of DEALS IPT9 GRPS</p> <p>= bits per unit u</p> <p>$CDMSA(m)$ of DEALS IPT9 GRPS</p> <p>= number of u units available on memory m</p>
<p>Example:</p> <p>MEMORY: M1 DEVICE: 32-MEM</p> <p>UNIT: 888 AMOUNT: 32768</p> <p>$L_m = 8 * 32768 = 262144$</p> <p style="margin-left: 100px;"> \nearrow TMAUP \nearrow CDMSA </p>			

MATH SYMBOL	DESIGN INTERMEDIATE	VALUE	DEFINITION AND RELATED PARAMETERS
I_{mb}	MBVAL(m,b) of IPT9 GRP10		<p>= length in bits of block b when stored in memory m</p> <p>= BLMR(b) maximum records</p> <p>* BLRW(b,3) maximum generic words/record</p> <p>* $\lceil \text{BLRBI}(b) \rceil$ ceiling of bits per byte } bits/word divided by = addressable unit which can best handle the load</p> <p>* BLRBY(b) bytes per word</p> <p>/TMAUP(k,u,2)]</p> <p>where</p> <p>$I = \lceil x \rceil$ = ceiling of x</p> <p>$x \rightarrow I$</p> <p>i.e., 0.9 1</p> <p>1.0 1</p> <p>1.1 2</p> <p>BLMR, BLRW, BLRBI, and BLRBY of IPT9 GRP11</p> <p>TMAUP(k,u,2) of IPT5 GRP5</p> <p>k is memory device associated with memory m</p> <p>u is addressable unit best suited</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
M	NM of IPT9 GRP2	Positive integer s NM of IPT9 GRP1	= number of memories This is accumulated by PASS1 in DEALS PPD 12, 13 ADDMM (add memory definition). In Sample Problem: 1 NM = 3 2 NM = 6

PAGE 22

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
N_t			<p>= number of times task t is to be executed during the evaluation interval τ for which partitioning is being done</p> <p>= $TAFRQ(t) * BLPER$</p> <p>where</p> <p>$TAFRQ(t)$ of IPT9 GRP12 is iteration of task t per sec</p> <p>$BLPER$ of IPT9 GRP13 is evaluation period in sec</p> <p>Sample Problem No. 2</p> <p>$TAFRQ(1)$ = iteration rate for task T1-3 = 30</p> <p>$BLPER$ = 1 sec</p> <p>N_t = $TAIT(t) * BLPER$</p>

MATH SYMBOL	DESIGN PHONETIC	VALUE	DEFINITION AND RELATED PARAMETERS
O_t		Nonnegative integer	<p>= number of distinct output data blocks for task t</p> $TANIO(t) = \sum_{o=1} f(TAHR(t,o))$ <p>where</p> $f(TAHR(t,o)) = \begin{cases} = 1 & \text{if } TAHR(t,o) = 2 \\ = 1 & \text{if } TAHR(t,o) = 1 \\ = 0 & \text{otherwise} \end{cases}$ <p>TAHR(t,o) and TANIO(t) are in IPT9 GRP12.</p>

ISSUE

DATE

ID

SEC

PAGE 24

MATH SYMBOL	DESIGN PNEUMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
0_{t0}	TAI08(t,i) of IPT9	Positive integer	= global data block index for task t output block o = TAI08(t,i) provided that TAI08(t,i) = 2 or 3 TAI08 of IPT9 GRP12

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
P	NP of IPT9 GRP2	Positive integer ≤ NP of IPT9 GRP1	<p>= number of processors</p> <p>NP is accumulated by PASS1 in DEALS PPD 1211 ADDPU (add processor unit definition).</p> <p>In sample problems</p> <p>No. 1 NP = 2</p> <p>No. 2 NP = 4</p>

ISSUE DATE ID SEC PAGE 26

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
Q	MQ of IPT9 GRP2	Positive Integer	= number of communication links MQ is accumulated in PASS1 by DEALS PPD 1212 ADDCL (add communication link).

ISSUE

DATE

ID

SEC

PAGE 27

AD-A096 456

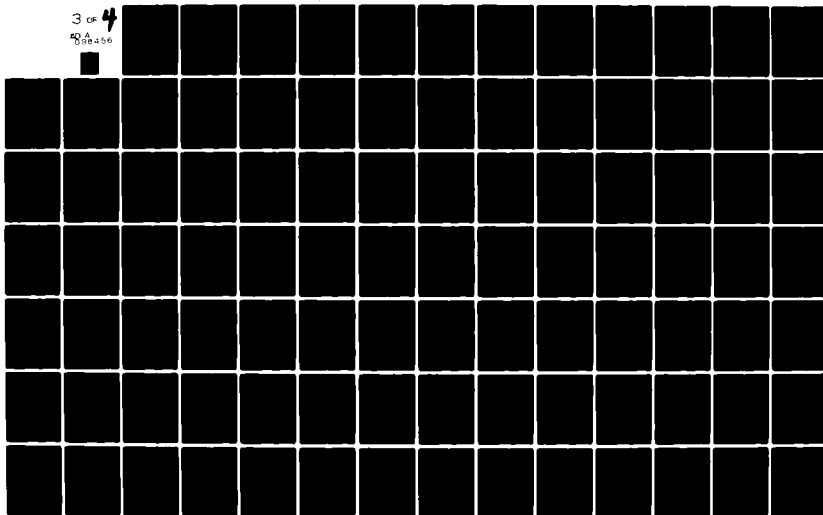
TELEDYNE BROWN ENGINEERING HUNTSVILLE ALA SYSTEMS DIV F/6 9/2
SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
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3 of 4
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MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
R_{tp}	TPOSH(p,9) of DEALS IOPT5 GRP3	Real	= resource task management coefficient for task t on processor p which is independent of enablement rate prorated for a second of processor time

ISSUE DATE ID SEC PAGE 28

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
r_{tp}		Real	<p>= resource task management per task t execution on processor p in seconds with accuracy to nanoseconds</p> <p>dependent on task enablement discipline</p> <p>if time enabled</p> <p>$r_{tp} = TPOSIM(p,4)$ of IOPT5 GRP3</p> <p>if data enabled</p> <p>$r_{tp} = TPOSIM(p,6)$ of IOPT5 GRP3</p> <p>if slaved</p> <p>$r_{tp} = TPOSIM(p,8)$ of IOPT5 GRP3</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
S_t	TAMET(t) of IPT9 GRP12	Real	= maximum time limit per task t execution in seconds with accuracy to microseconds

ISSUE

DATE

ID

SEC

PAGE 30

MATH SYMBOL	DESIGN Mnemonic	VALUE	DEFINITION AND RELATED PARAMETERS
S_{mb}	MBMAP(m,b,1) of IPT9 GRP10	0,1	<p>= 1 if memory storage m contains block b</p> <p>= 0 otherwise</p> <p>This is a major output of PASS2 and PASS3.</p>

ISSUE DATE ID SEC PAGE 31

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
T	NT of IPT9 GRP2	Positive integer ≤ NT of IPT9 GRP12	= number of tasks to be allocated to processors NT is accumulated by PASS1 DEALS PPD 1320 ADDTSK (add task definition).

PAGE 32

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
τ	BLPER of IPT9 GRP13	REAL > 0	= time period for which partition is being allocated in seconds

PAGE 33

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN NOMECLATIC	VALUE	DEFINITION AND RELATED PARAMETERS
U_p	CDPCU(p) of IPT9 GRP4	Positive real	<p>= current allocation utilization estimate for processor p</p> <p>= $\frac{1}{T} \sum_{t=1}^T [(c_{tp} + r_{tp}) e_{tp}]$ task computation and resource management time</p> <p>+ $\sum_{i=1}^{I_t} A_{ti} \sum_{m=1}^m r_{mp}^{-1} r_{mti} a_{mpti}$ task input processing</p> <p>+ $\sum_{o=1}^{O_t} \alpha_{to} \sum_{m=1}^M \omega_{mp}^{-1} \omega_{mto} w_{mpto}$ task output processing</p> <p>+ $R_{tp} x_{tp}]$ task resource management</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
u_m	CMCU(m) of IPT9 GRPS	Positive real	<p>= current partition solution estimate for memory m's allocated storage</p> $= \frac{1}{L_m} \sum_{b=1}^B l_{mb} s_{mb}$

ISSUE DATE ID SEC PAGE 35

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
v_{mpto}	MP SOL (m, p, e, 4)	Nonnegative integer	<p>= the number of times output block o of task t is written or updated by task t on processor p to memory m</p> <p>This is a function of the current partition variables</p> <p>TPMAP(t, p, 1) of DEALS IPT9 GRP8 MPMAP(m, p, 1) of DEALS IPT9 GRP9 MBMAP(m, b, 1) of DEALS IPT9 GRP10</p> <p>where b = TAI08(t, 0) of DEALS IPT9 GRP12 block b is either an update or output (i.e., TAI08(t, 0) = 2 or 3 in DEALS IPT9 GRP12)</p> <p>Actual automated implementation should consider a function or subroutine for current partitioning decision and measures. If block b is stored in replicate locations, this becomes more complex.</p>

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
w_{mp}		0,1	<p>= 1 if processor p is permitted to change contents memory m; i.e., there is at least one write access link q from p to m</p> <p>= 0 if otherwise</p> <p>w_{mp} can be computed as follows:</p> <p>= 1 if $MPMAP(m,p,2) > 0$</p> <p>= 0 otherwise</p> <p>$MPMAP(m,p,2)$ of IPT9 GRP9</p>

PAGE 37

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
Ω_{to}	TARWF(t,o) of IPT9 GRP12	Positive real	<p>= percent of information output from task t to block o dependent on task/block evaluation level: minimum, average, worst-case (k = 1, 2, 3, respectively)</p> <p>$TARWF(t,o) = TARW(t,i,k)/BLMXR(b)$</p> <p>where</p> <p>$TARW(t,i,k)$ is in IPT9 GRP12 and is set by PASS1 DEALS PPD 1630 PACLC.</p>

ISSUE

DATE

ID

SEC

PAGE 38

MATCH SYMBOL	DESIGN MNEMONIC	VALUES	DEFINITION AND RELATED PARAMETERS
ω_{mp}	MPMAP (m,p,2) of IPT9 GRP9	Real ≥ 0	= bits/sec transfer rate from processor p to memory m based on statistical composite of write access links for p and m.

PAGE 33

SEC

ID

DATE

ISSUE

MATH SYMBOL	DESIGN ANEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
x_{tp}		0,1	<p>= 1 if task is assigned to execute on processor p = 0 otherwise</p> <p>x_{tp} is a function of the current partition solution as follows: = 1 if $TPMAP(t,p,1) > 0$ = 0 otherwise</p> <p>where $TPMAP$ is in IPT9 GRP8</p>

ISSUE

DATE

ID

SEC

PAGE 40

MATH SYMBOL	DESIGN MNEMONIC	VALUE	DEFINITION AND RELATED PARAMETERS
y_{tp}			<p>= duplicate development cost to implement task t on processor p as currently partitioned if task t is on more than one processor</p> <p>= 0 for $p = 1$</p> <p>= maximum ($\lambda_{ipt} x_{ti}$ for $i = 1$ to $p - 1$) for $p > 1$</p> <p>where</p> <p>$\lambda_{ipt} = 1$, if common language available on processor i and p ($i \neq p$) for task t</p> <p>= .25 if different languages are to be used ($i \neq p$)</p> <p>= 0 if $i = p$.</p> <p>Other values may be assigned as a function of the master language list. Note this is the amount by which development cost is reduced due to duplicate effort not needed for additional processors.</p>

ISSUE

DATE

ID

SEC

PAGE 41

SAMPLE PROBLEM OUTPUT FORMAT 1

MM/DD/YY	HH:MM:SS	EVALUATION	GLOBAL PARTITION	EX	CANDIDATE	SAMPLE CONFIGURATION	PASS PAGE	1
SYSTEM INTERFACE DEFINITION		TECHNOLOGY HYPOTHETICAL		TECH DB	SOFTWARE SAMPLE APPLICATION			

C.4 SAMPLE OUTPUTS

FORMAT 1. STANDARD RUN IDENTIFICATION

SAMPLE PROBLEM OUTPUT FORMAT 2

HARDWARE COMPONENT SUMMARY

CATEGORY/DEVICE	IDENTIFIER	REQUIRED
PU 86-PROC	A	YES
PU SPC	SPC	YES
PU XYZ32/75	A1	CAND
PU XYZ32/75	B1	CAND
MM 86-MEM	M6	YES
MM 32-MEM	M1	CAND
MM 32-MEM	M2	CAND
MM 32-MEM	M3	CAND
MM 32-MEM	M4	CAND
MM 32-MEM	M5	CAND
CL ASYNC-IO	EIO-1	YES
CL ASYNC-IO	EIO-2	YES
CL M7LINK-86	EIO-3	YES
CL HSD	EIO-4	YES
CL MBUS	C1	CAND
CL MBUS	C2	CAND
CL MBUS	BUS2	CAND
CL MBUS	BUS1A	CAND
CL MBUS	BUS1B	CAND
CL HSD	HSD	CAND
CL 86MBUS	BUS3	CAND

SAMPLE PROBLEM OUTPUT FORMAT 3

DATA BLOCK SUMMARY AND EXTERNAL SOURCE/DESTINATION

BLOCK	IDENTIFIER	LEVEL -FLAG	DISCIPLINE -FLAG	MAXIMUM RECORDS	BITS/ BYTE	BYTES/ WORD	WORDS-PER-RECORD MIN AVE MAX	EXTERNAL COMPONENT IDENTIFIER	FREQUENCY
1	PAOL	S	RAN	128	8	4	1 1 1		
2	DIRLITE	S	RAN	256	8	4	1 1 1		
3	CAOUT	S	CBUF	2	8	4	128 128 128	HSD	30
4	A0BJL	S	RAN	100	8	4	1 1 1	HSD	30
5	MOOPLIST	S	RAN	20	8	4	1 1 1	HSD	30
6	CAIPT	S	CBUF	2	8	4	128 128 128	HSD	30
7	DYNDATA	S	RAN	8192	8	4	1 1 1	HSD	30
8	SIMPOS	S	CBUF	2	8	4	128 128 128	ET0-4	30
9	RANPOS	S	CBUF	2	8	4	128 128 128		
10	G1	G	RAN	1024	8	4	1 1 1		
11	ADATA	G	RAN	512	8	4	1 1 1		
12	B0DATA	G	RAN	512	8	4	1 1 1		
13	BOMB0DATA	L	RAN	512	8	4	1 1 1		
14	DYNDATASH	S	RAN	1	8	4	1 1 1	AIS	30

SAMPLE PROBLEM OUTPUT FORMAT 4

TASK SUMMARY

TASK	IDENTIFIER	LANGUAGE	INPUT BLOCKS	OUTPUT BLOCKS	ENABLEMENT DISCIPLINE	FREQ 1	FREQ 2	FREQ 3
1	T13	ASSEMBLER	SIMPOS RAWPOS DIRLITE G1	DIRLITE PAOL G1 DYNDATA	TIME	30		
2	T46	FORTRAN IV G1	G1	CAIPT	SLVD		30	
3	A713	FORTRAN IV G1	ADATA	DYNDATA ADATA	SLVD		30	
4	B7-13	FORTRAN IV G1	BDATA	DYNDATA BDATA	SLVD		30	
5	T14&16	FORTRAN IV G1	BOMBDATA	BOMBDATA	SLVD		30	
6	T15	MACRO ASM	DYNDATA	DYNDATA	SLVD			30
7	T17-19	FORTRAN IV	CAOUT AOBJL MODPLIST	AOBJL MODPLIST	DATA			30

SAMPLE OUTPUT FORMAT 6 (Sheet 1 of 2)

EVALUATION ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE	COMPONENT ASSIGNED	APPLICATION COMPONENT IDENTIFIER	CONFIGURATION COMPONENT IDENTIFIER	VALUE WHEN APPLICABLE
Fixed	Task	T1-3	A1	30
Initial	Task	T4-5	A1	30
Initial	Task	A7-13	A1	30
Initial	Task	T17-19	A1	30
Prohibited	Task	T17-19	B1	30
Initial	Task	87-13	B1	30
Initial	Task	T14&16	B1	30
Initial	Task	T15	B1	15
Initial	Task	T15	A1	15
Fixed	Data	PAOL	M3	15
Fixed	Data	DIRLITE	M3	
Fixed	Data	CAOUT	M4	
Fixed	Data	A0BJL	M3	

SAMPLE OUTPUT FORMAT 6 (Sheet 2 of 2)

EVALUATION ASSIGNMENT CONSTRAINTS

ASSIGNMENT TYPE	COMPONENT ASSIGNED	APPLICATION COMPONENT IDENTIFIER	CONFIGURATION COMPONENT IDENTIFIER	VALUE WHEN APPLICABLE
Fixed	Data	MODPLIST	M3	
Fixed	Data	CAIPT	M4	
Fixed	Data	DYNDATA	M3	
Fixed	Data	SIMPOS	M1	
Fixed	Data	RAWPOS	M1	
Fixed	Data	G1	M3	
Initial	Data	ADATA	M1	
Initial	Data	BDATA	M2	
Initial	Data	BOMBDATA	M3	
Fixed	Data	DYNDATASW	M3	

EVALUATION PRIORITIES

360

SAMPLE PROBLEM OUTPUT FORMAT 8

BASIC PARTITIONING PROBLEM SIZE

7 TASKS	4 PROCESSORS
14 DATA BLOCKS	6 MEMORIES
2 PRIORITIES SELECTED	

SIMPLIFIED PROBLEM OUTPUT FORMAT 101

PRIORITY GOAL SUMMARY									
MAJOR PRIORITIES			PRIORITY COMPONENTS						
LEVEL	PRIORITY IDENTIFIER/ UNITS	GOAL/ TOLERANCE	CURRENT ACHIEVEMENT LEVEL / FLAG	COMPONENT	GOAL PERCENT	TOLERANCE	CURRENT ACHIEVEMENT LEVEL / FLAG		
1	PROCESSOR UTILIZATION % BUSY	60.00	60.00	P1	60	5.00	60		
		5.00%		P2	60	5.00	60		
2	DEVELOPMENT COST MANYEARS	5.00	5.60	T1	.5	10.00	.5		
		10.00%	**	T2	1.0	10.00	1.0		
				T3	1.0	5.00	1.5		
				T4	.5	1.00	.5		
				T5	2.0	10.00	2.0		
3	MEMORY UTILIZATION % ASSIGNED	60.00	53.00	M1	60	5.00	66.00		
		5.00%		M2	30	2.00	32.00		
				M3	60	5.00	59.00		

SIMPLIFIED PROBLEM OUTPUT FORMAT 102

TASK ALLOCATION									
TASK	PROCESSOR	EXECUTIONS	TOTAL TIME	FLAG	BLOCK	MEMORY	INPUT	OUTPUT	
T1	P1	20/20	.20		I1 B1 G1 S1 S2	M1 M1 M2 M1 M2	✓ ✓ ✓ ✓ ✓	✓	
T2	P1	10/10	.20		I2 G1 G2 S1	M1 M2 M2 M1	✓ ✓ ✓ ✓	✓	
T3	P2	20/20	.20		I3 G1 G3	M3 M2 M2	✓ ✓ ✓	✓ ✓	
T4	P1	20/20	.20		S2 I4 B2 G2 G3	M3 M2 M1 M1 M2 M2	✓ ✓ ✓ ✓ ✓ ✓	✓	
T5	P2	20/20	.40		I5 B3 G3	M3 M2 M3	✓ ✓ ✓	✓ ✓	

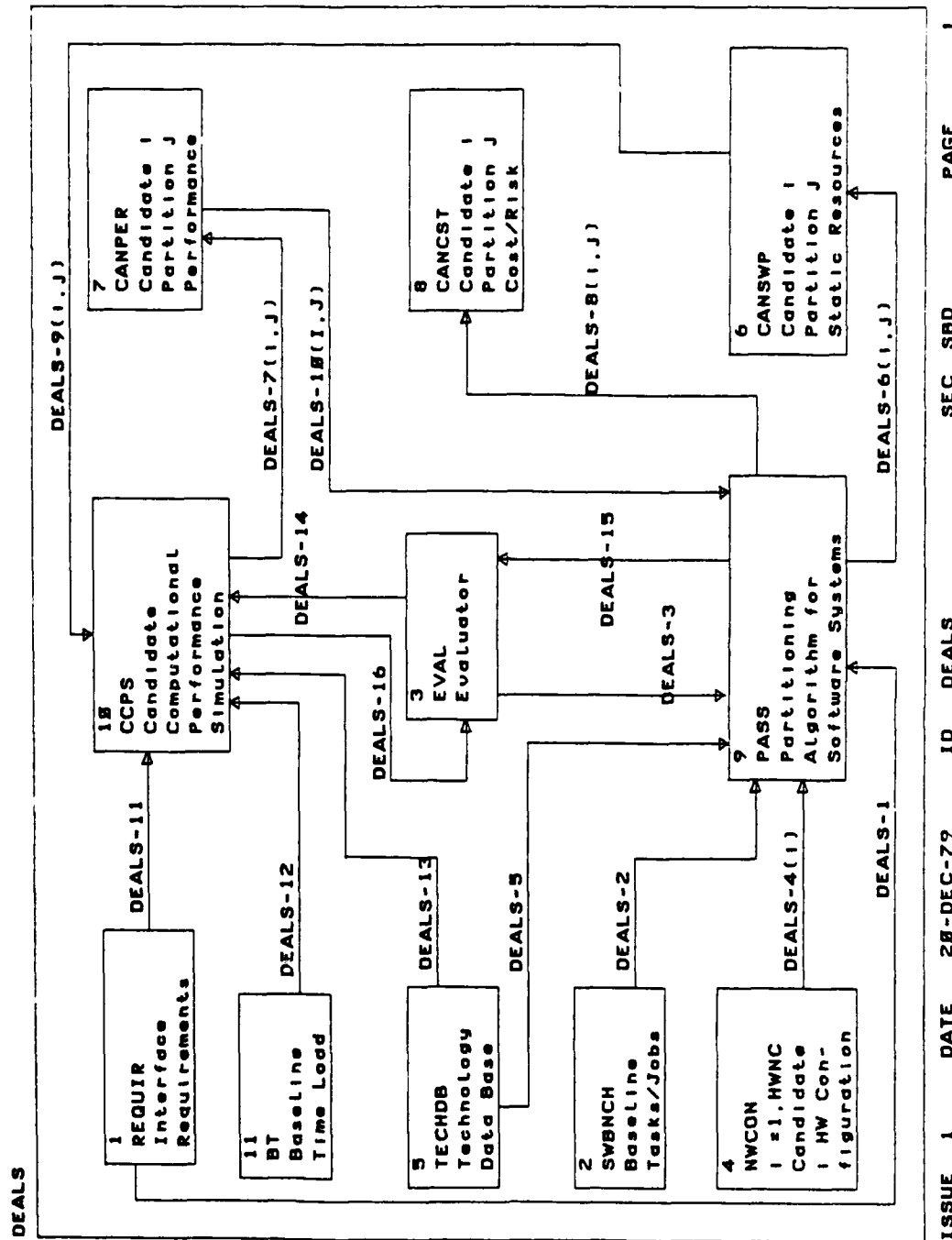
SIMPLIFIED PROBLEM OUTPUT FORMAT 103

DATA BLOCK ALLOCATION

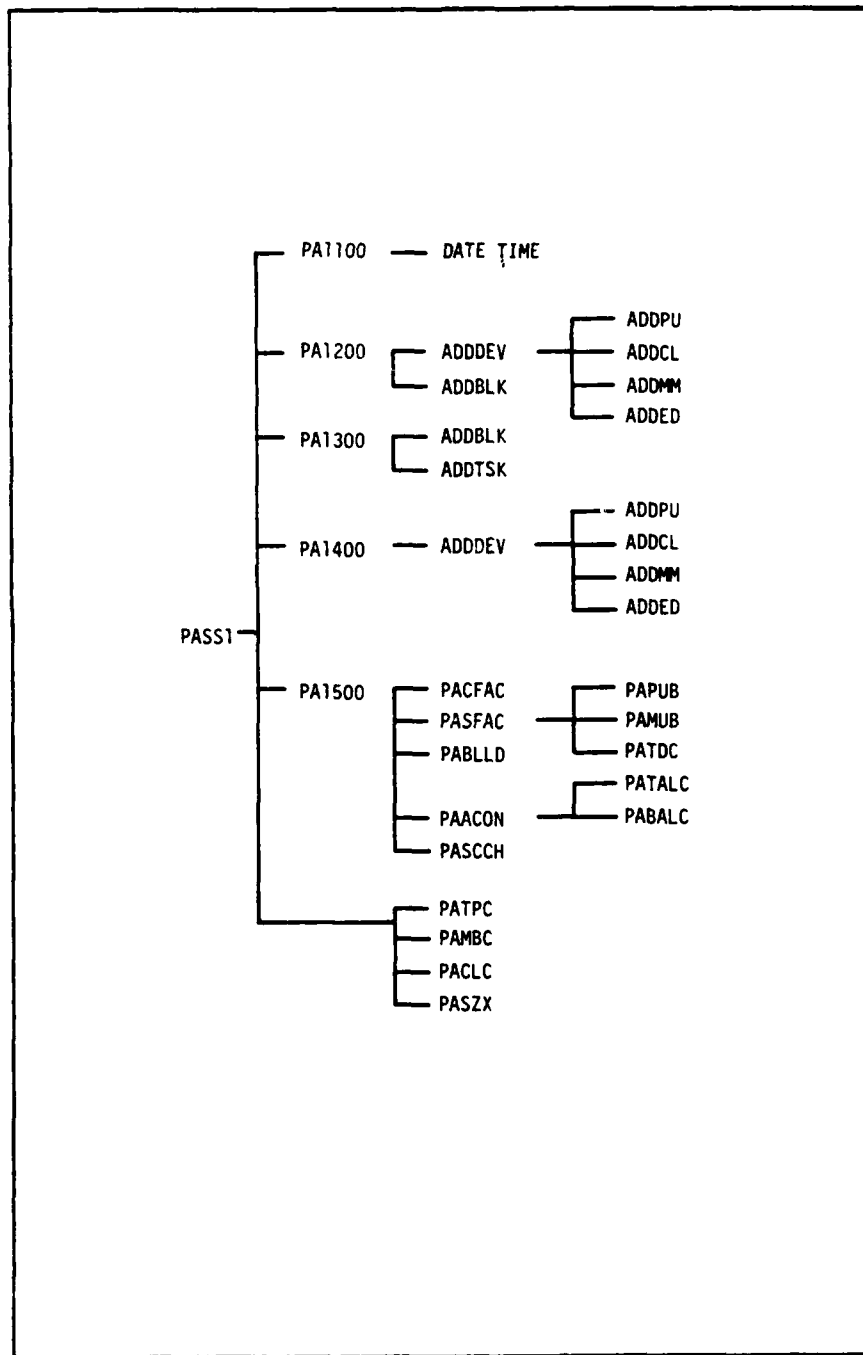
BLOCK	MEMORY	LENGTH	PERCENT	PROCESSOR	STORES	FETCHES	TOTAL	FLAG
B1	M1	1000	3.1	P1		500		
B2	M1	2000	6.2	P1	1000			
B3	M2	4000	12.5	P2	2000			
G1	M2	4000	12.5	P1	✓	✓		
				P2		✓		
G2	M2	1000	3.1	P1	✓	✓		
G3	M2	1000	3.1	P1		✓		
				P2	✓			
	M3	1000	3.1	P2	✓	✓		
S1	M1	256	.8	P1	✓	✓		
S2	M2	256	.8	P1	✓			
				P2		✓		
I1	M1	2000	6.2	P1	✓	✓		
I2	M1	12000	37.8	P1	✓	✓		
I3	M3	8000	25.0	P2	✓	✓		
I4	M1	4000	12.5	P1	✓	✓		
I5	M3	10000	31.2	P2	✓	✓		

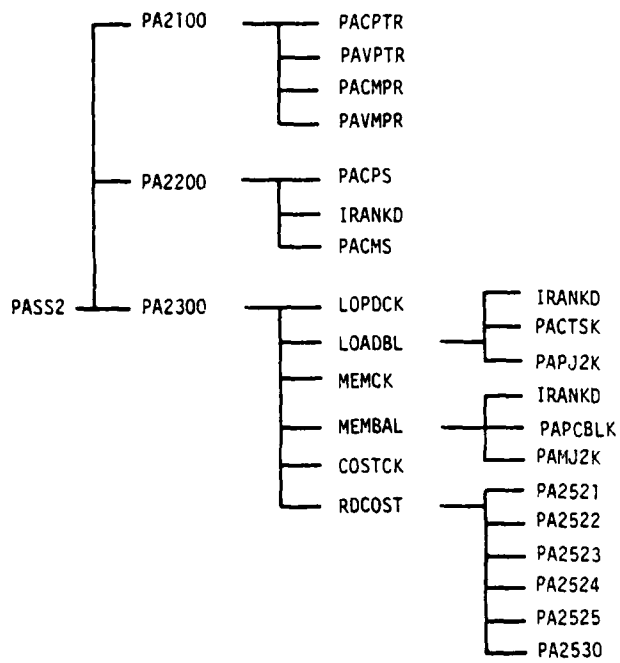
APPENDIX D.
DETAILED DESIGN

D.1 SYSTEM INTERFACE



D.2 HIERARCHICAL STRUCTURE





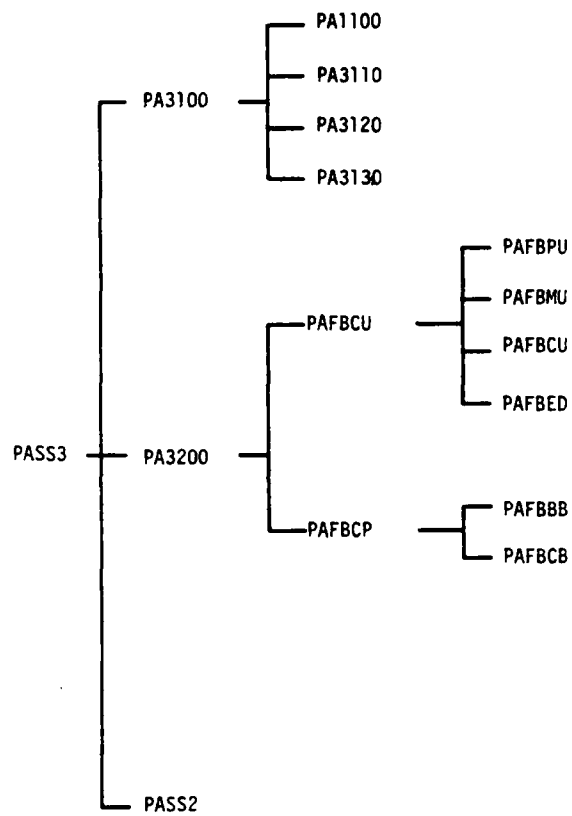
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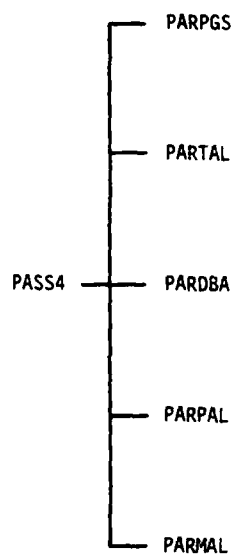
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PAGE

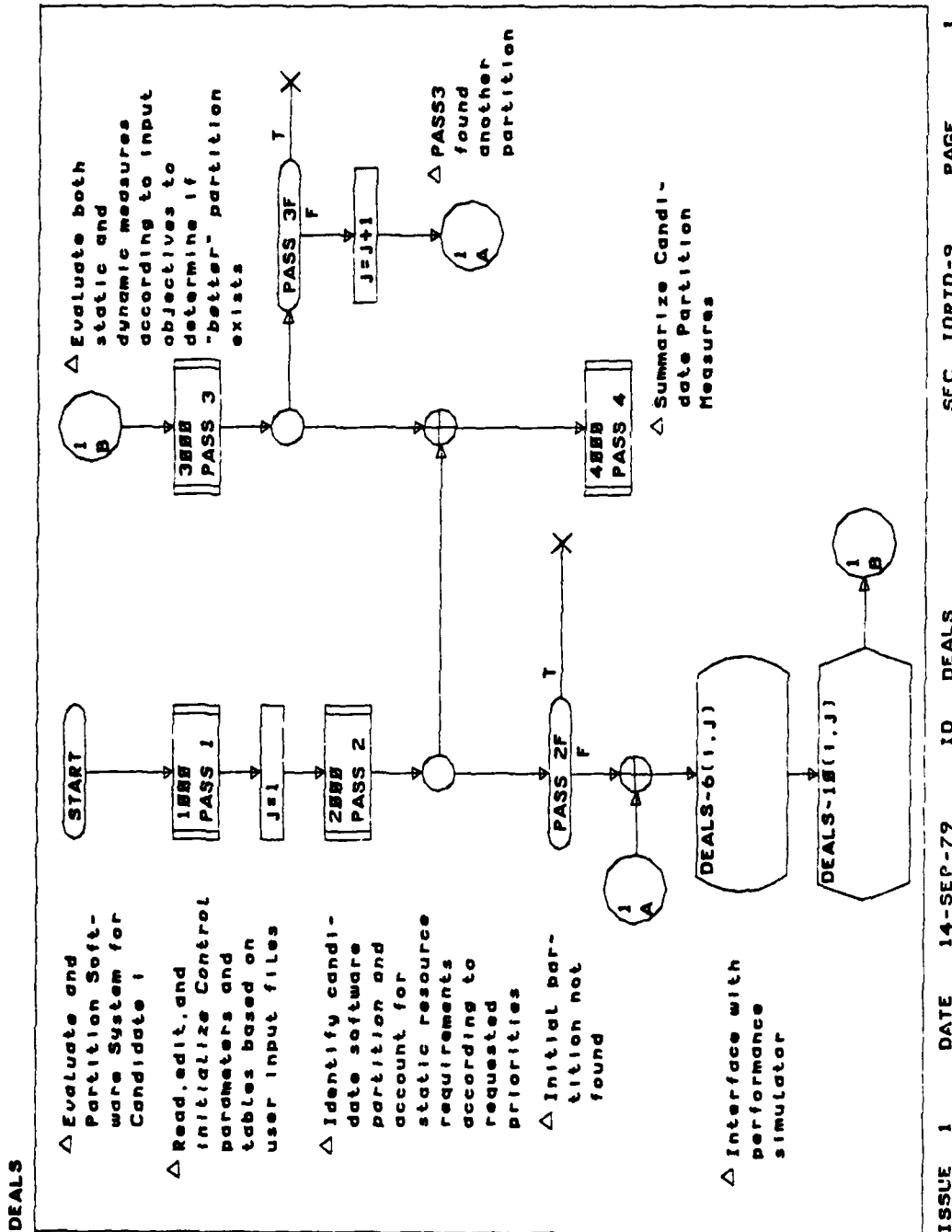
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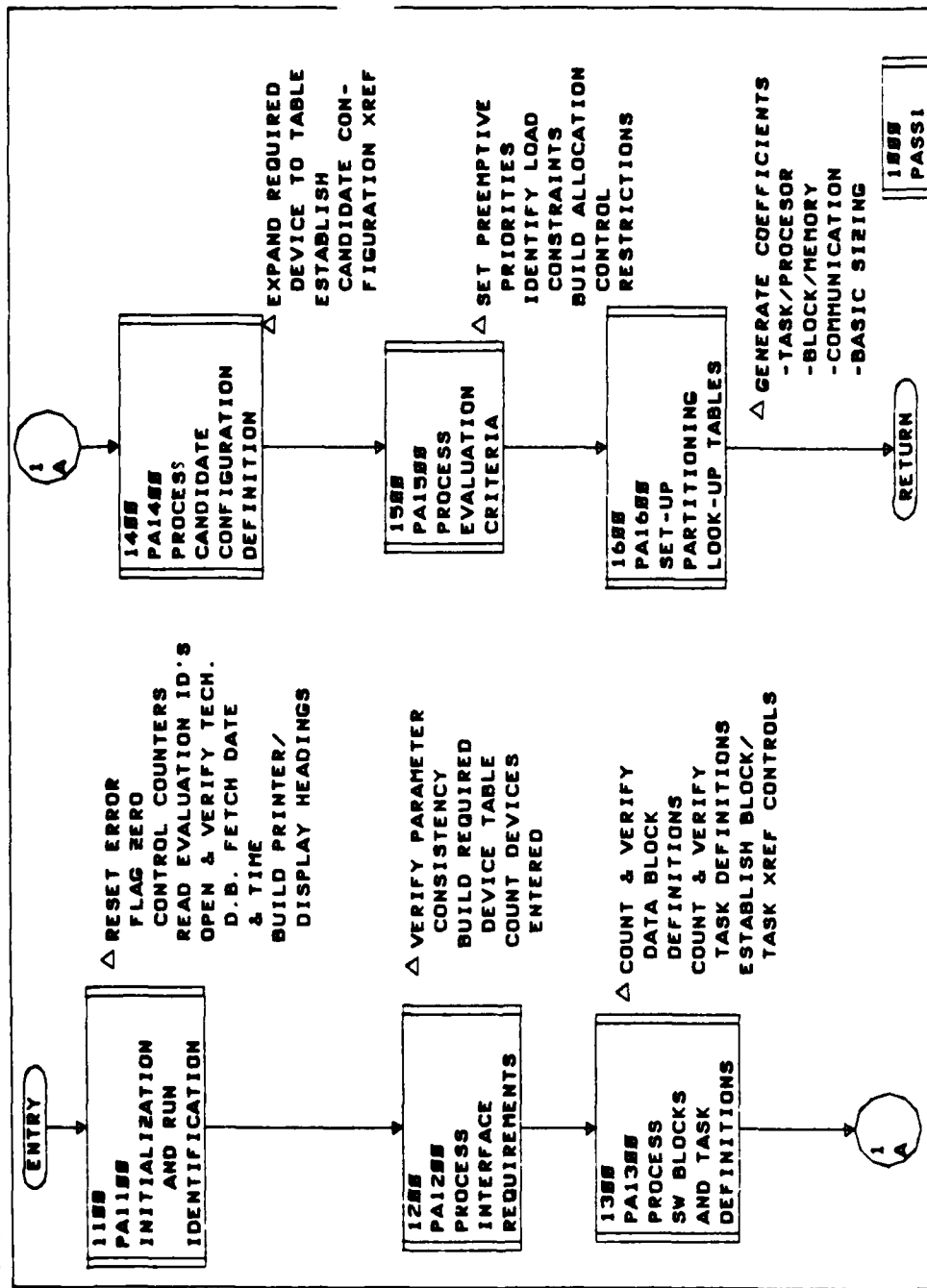
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ISSUE

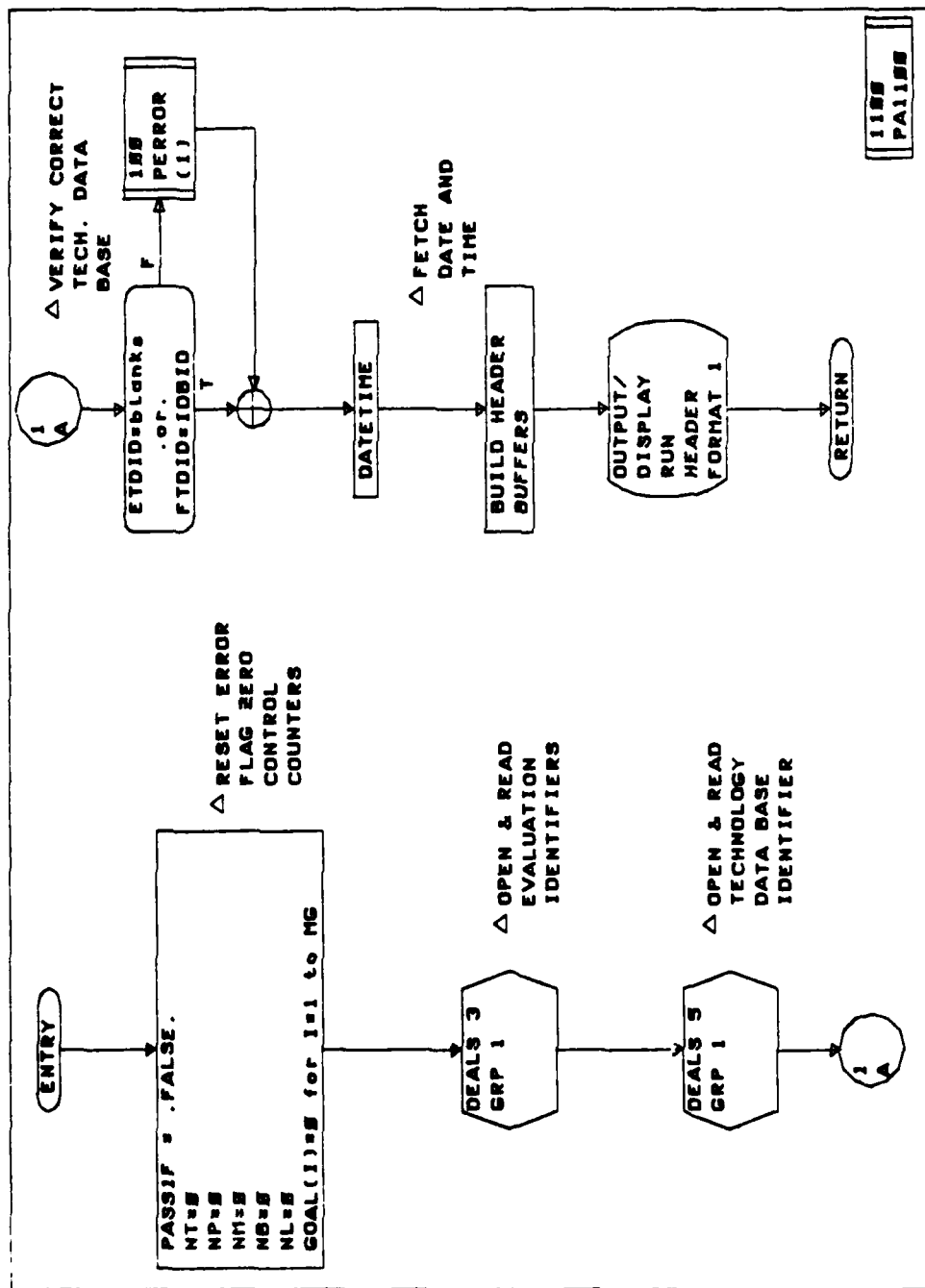
D.3 FLOW DIAGRAMS



DEALS

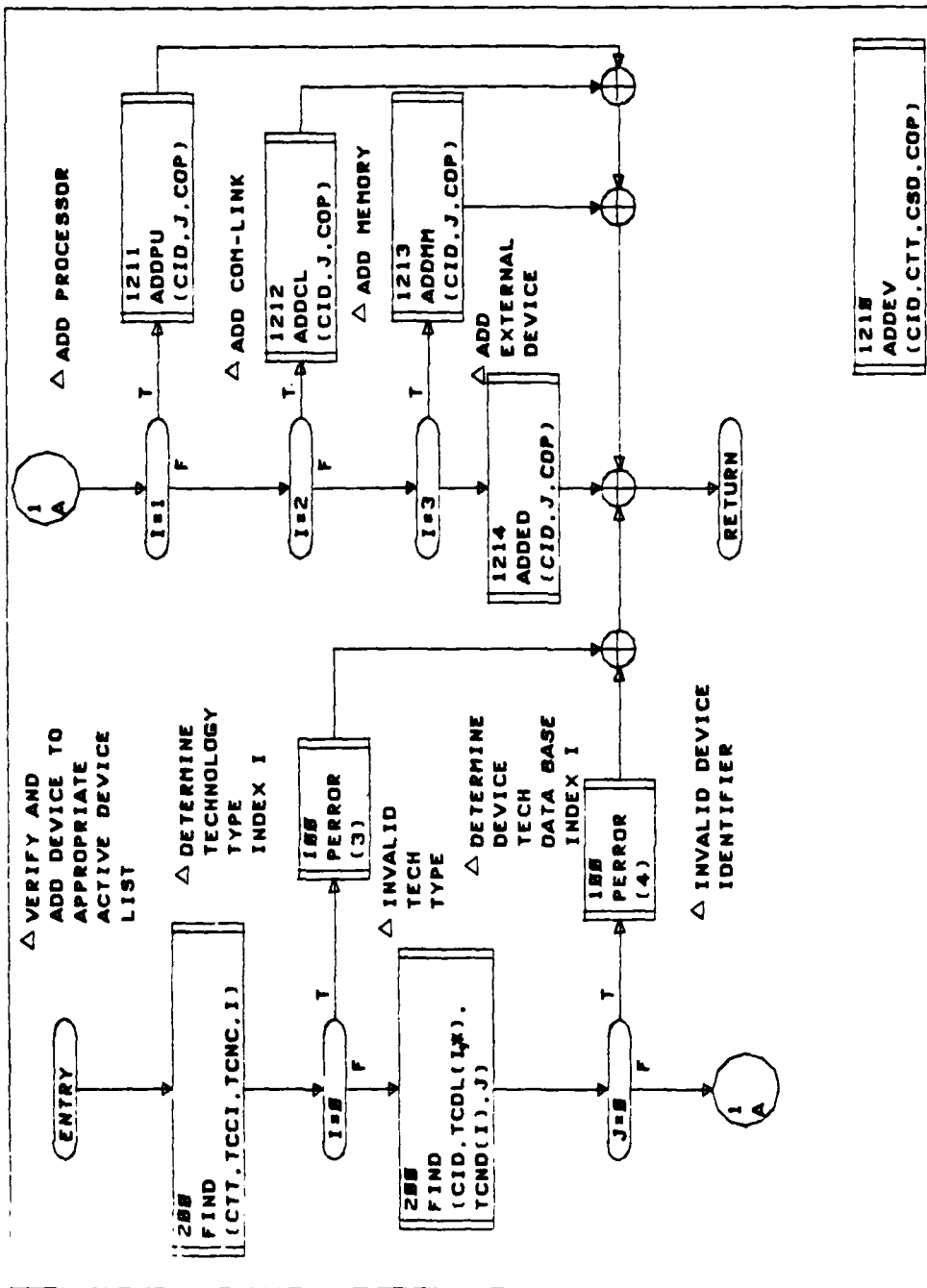


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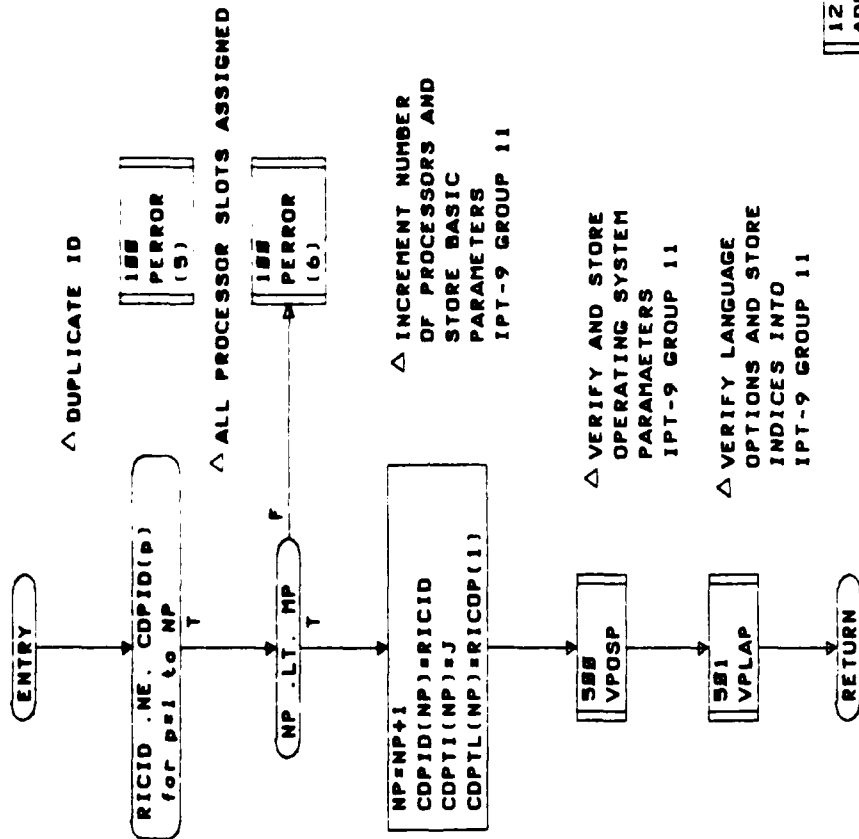


ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-1188 PAGE 1

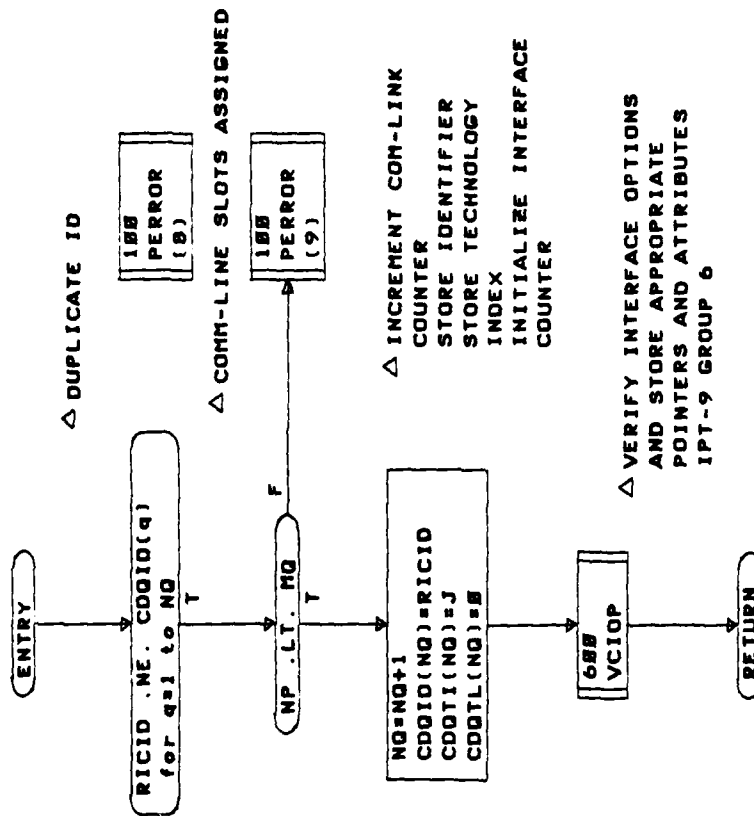




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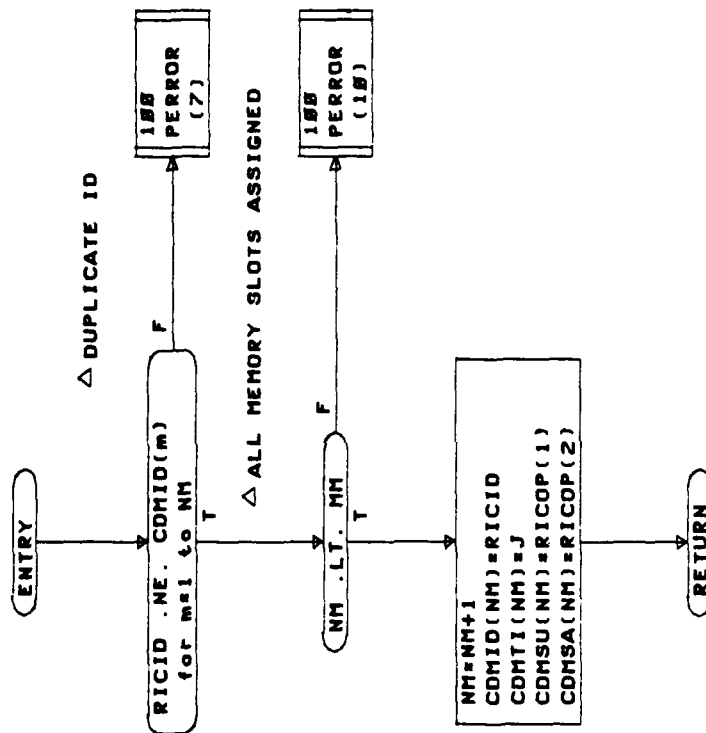


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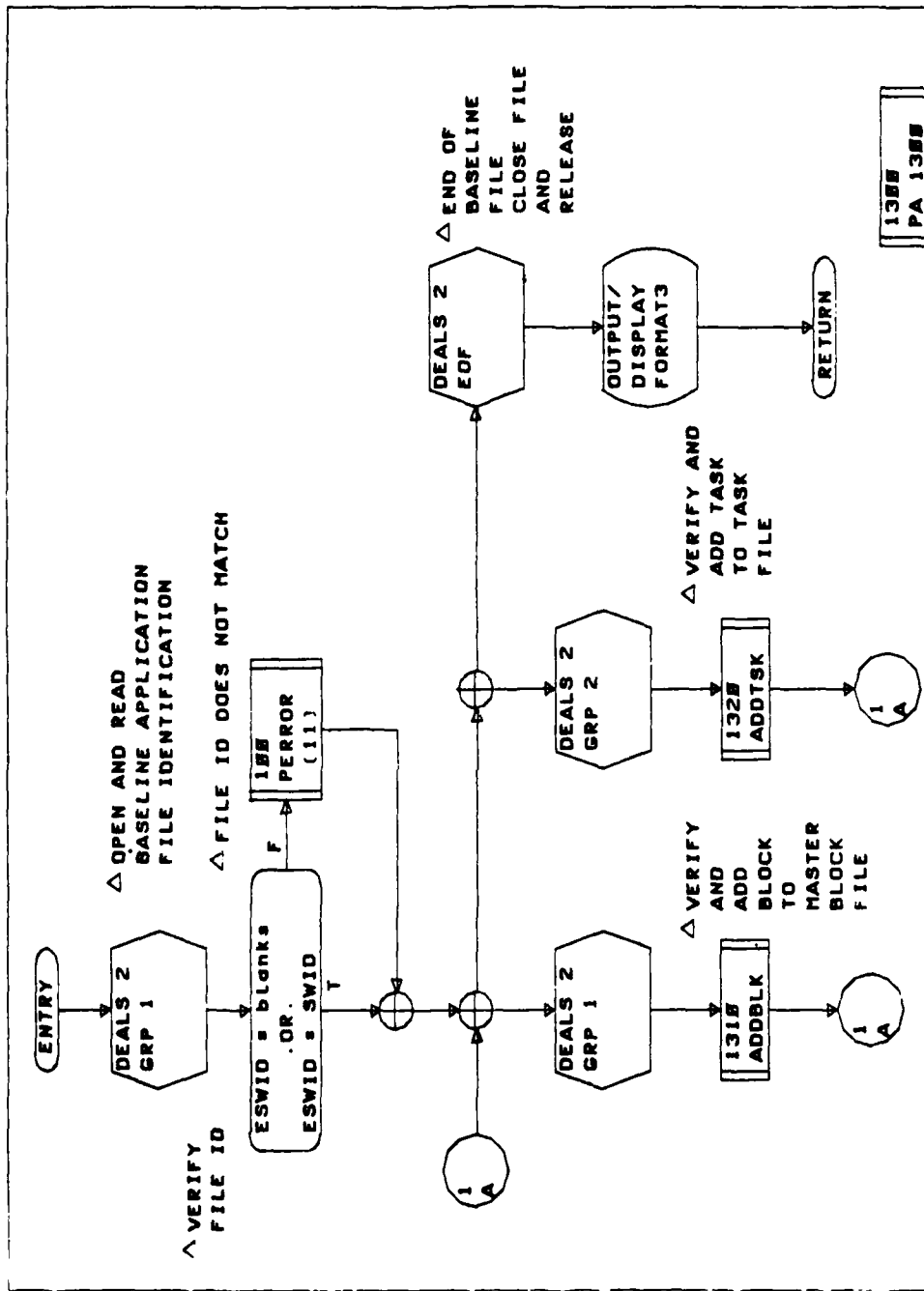
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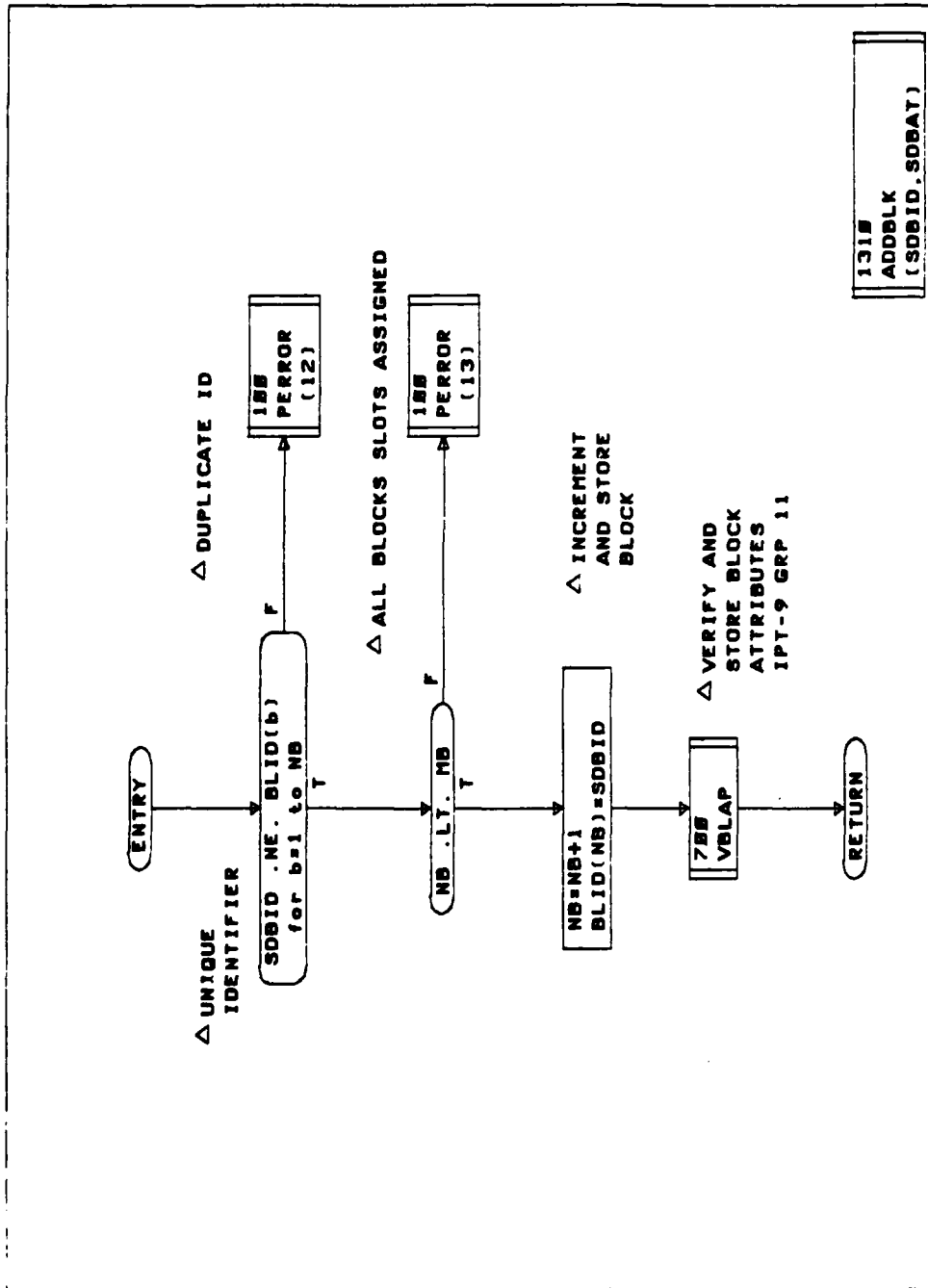
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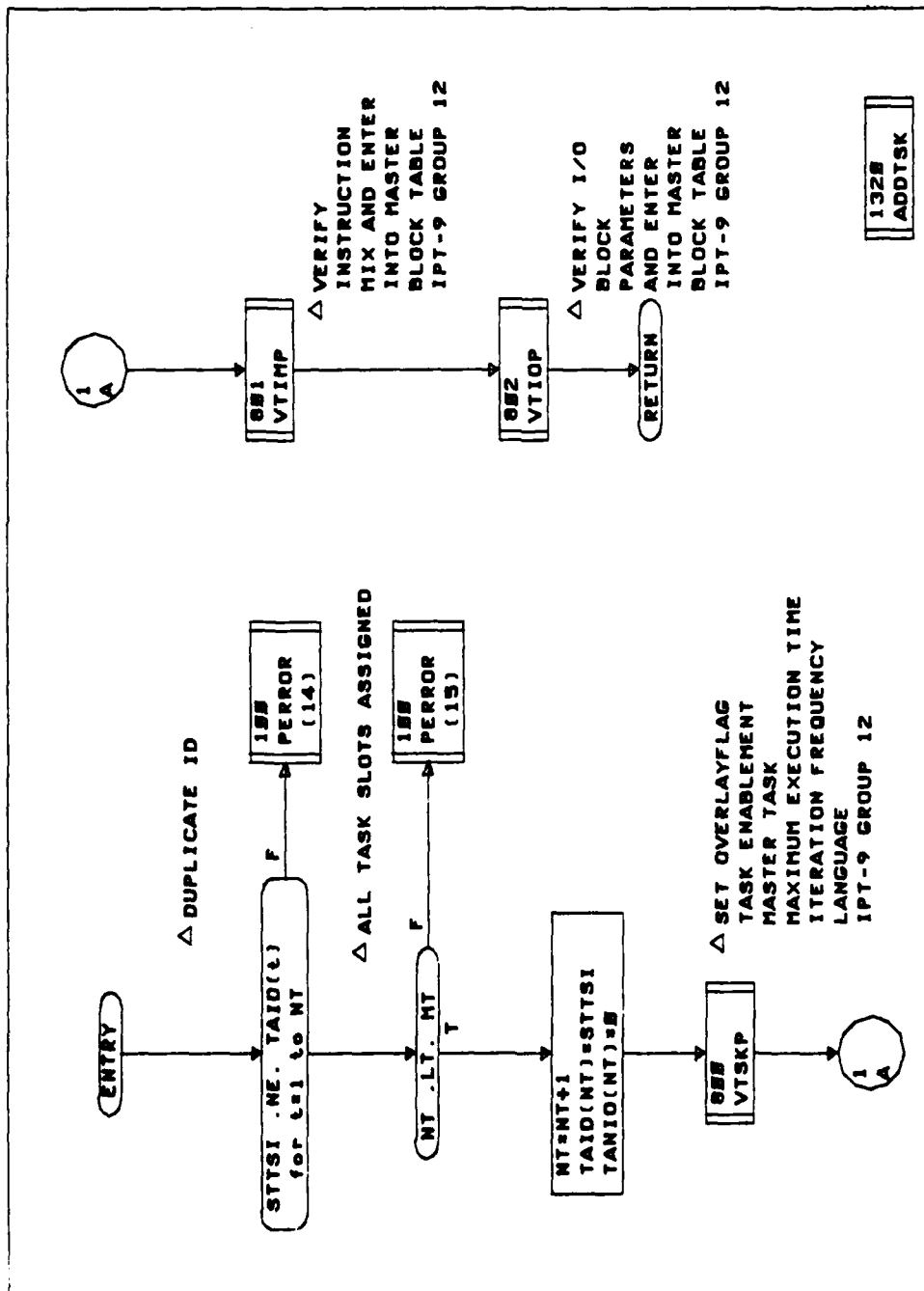


138B
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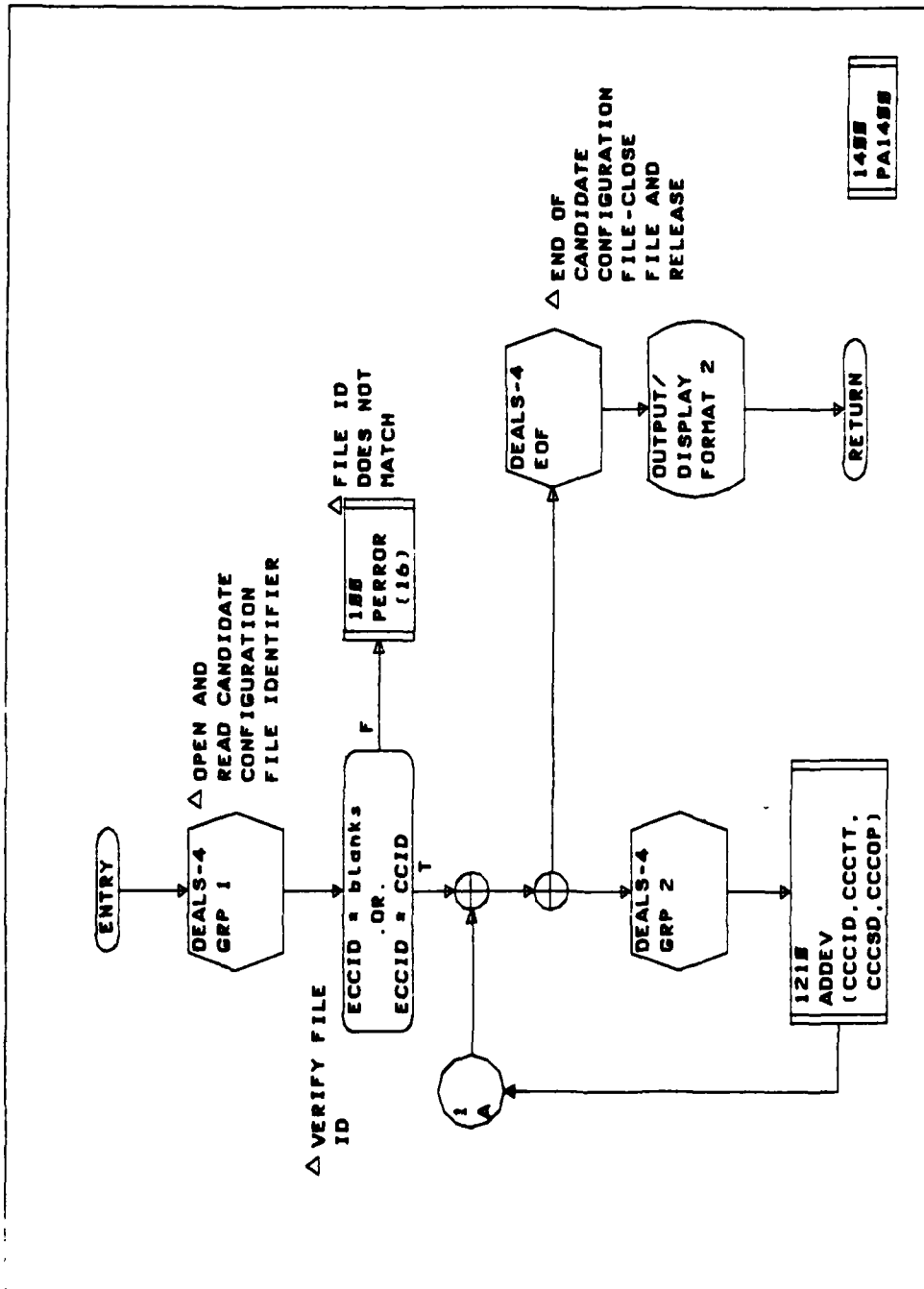
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DEALS

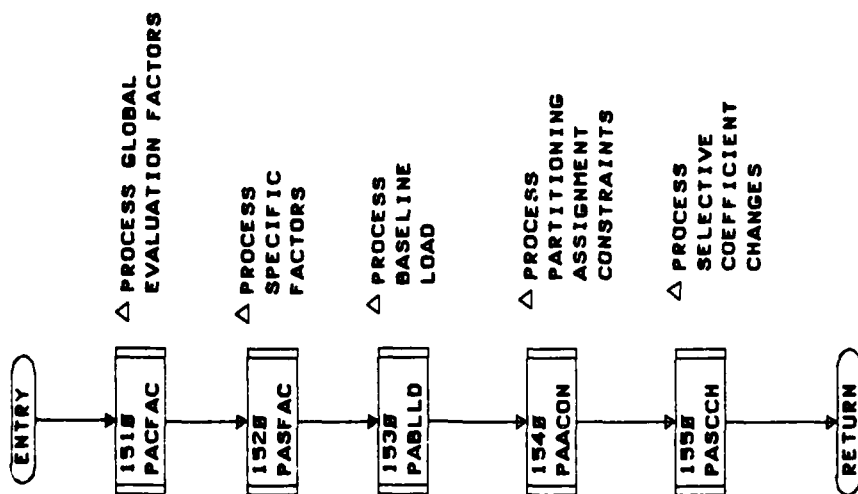


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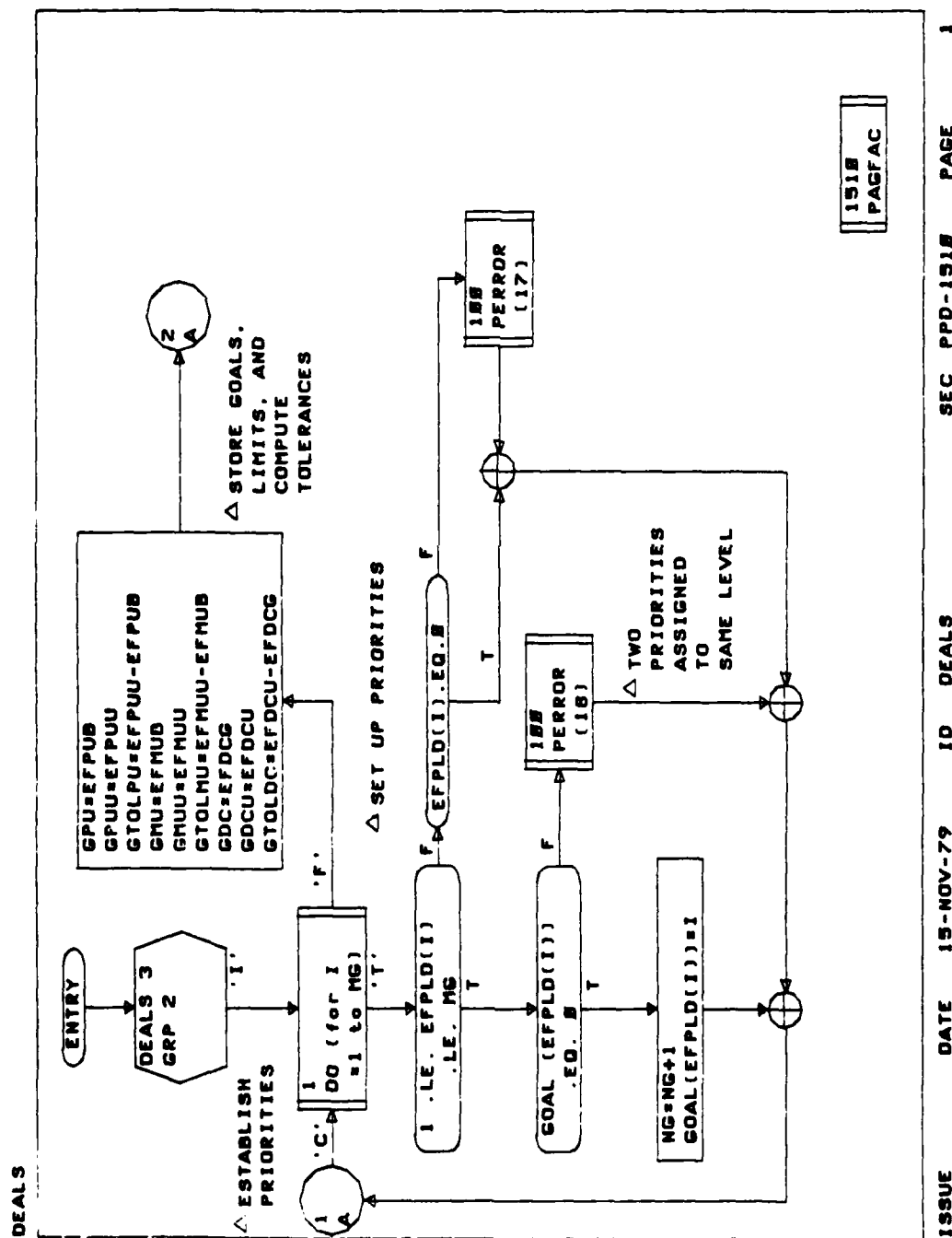
ISSUE DATE 15-NOV-79 ID DEALS SEC PPD-1488 PAGE 1

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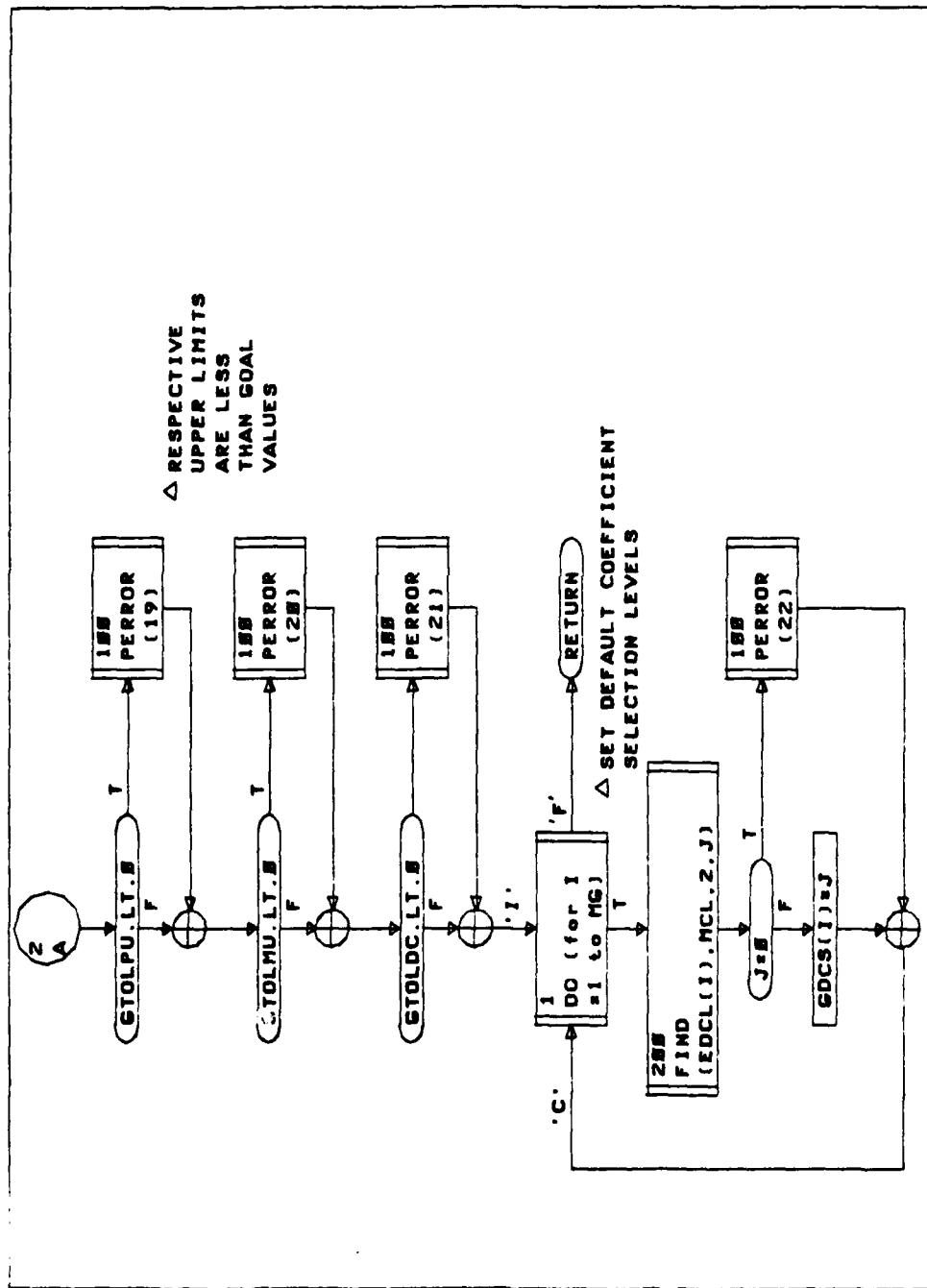


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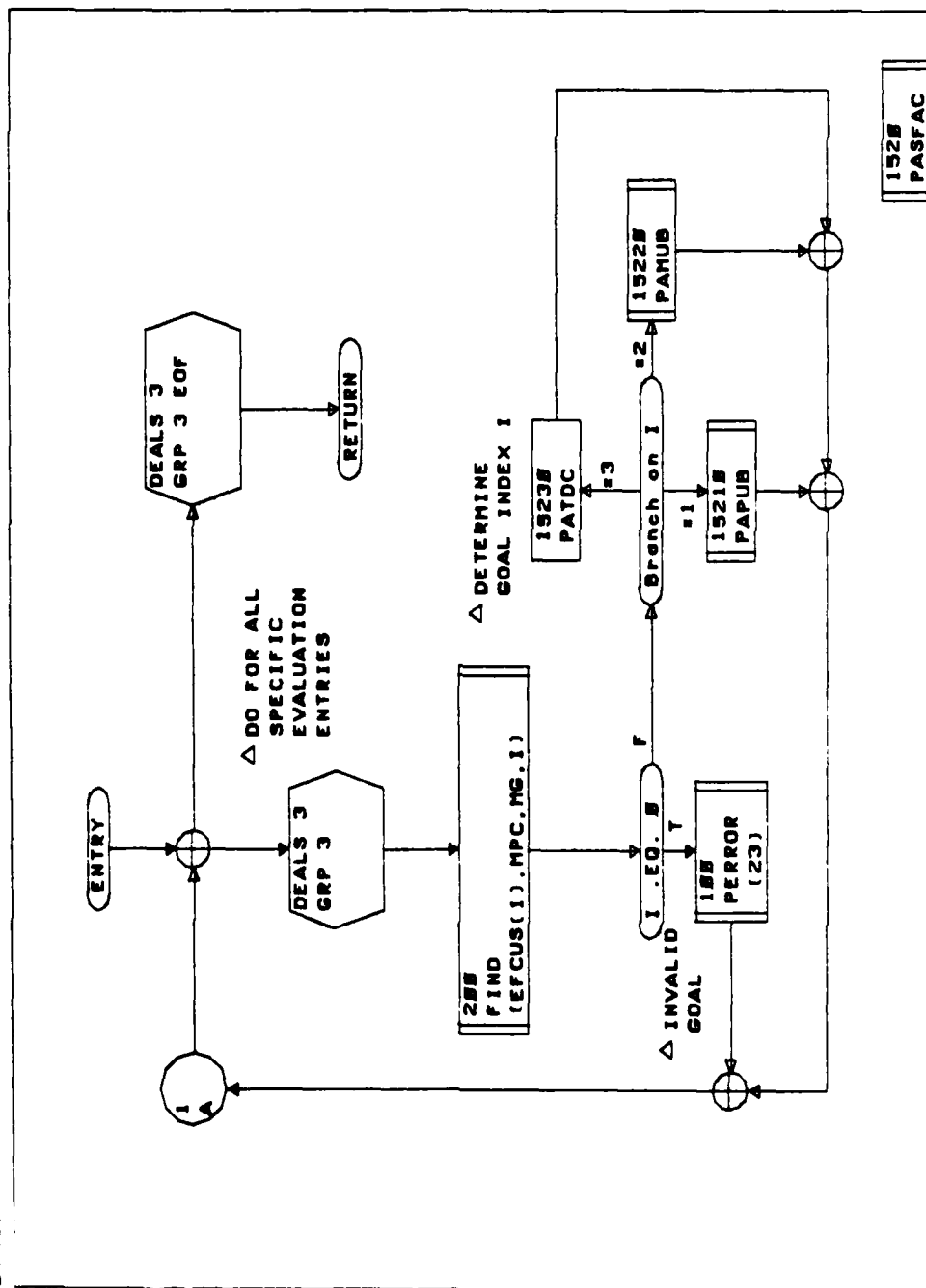
ISSUE DATE 14-NOV-79 ID DEALS SEC PPD-155B PAGE 1



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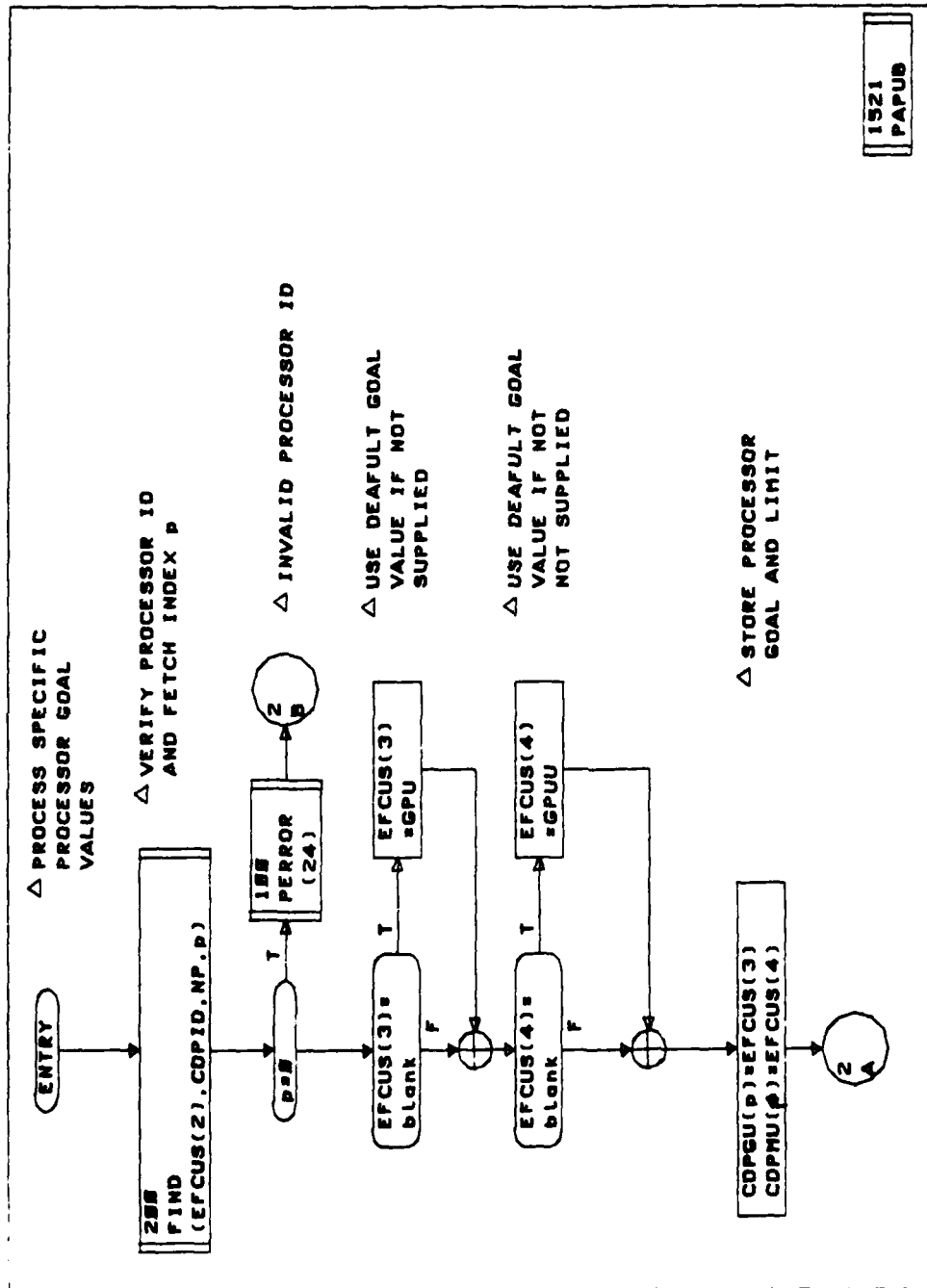


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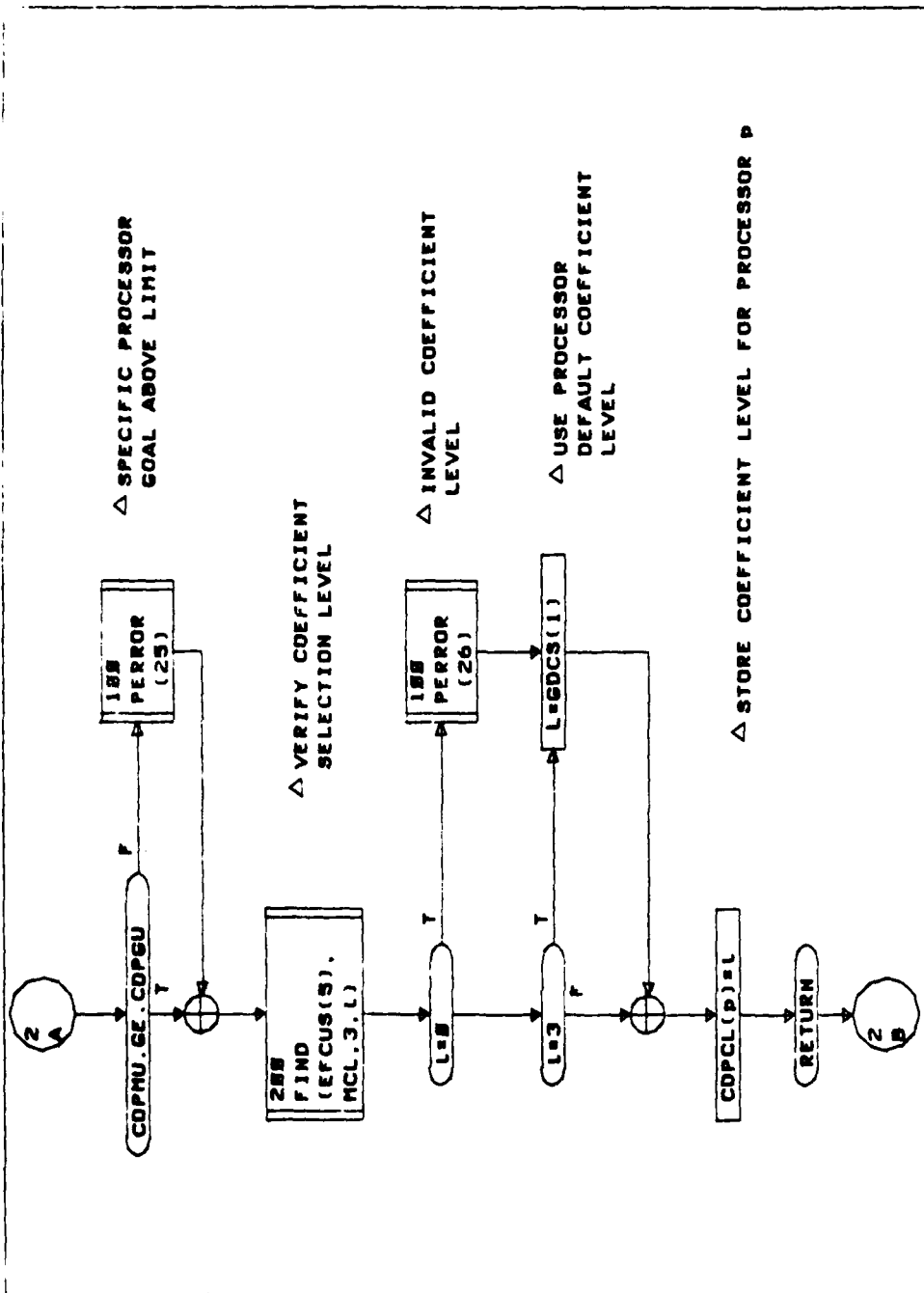


152B
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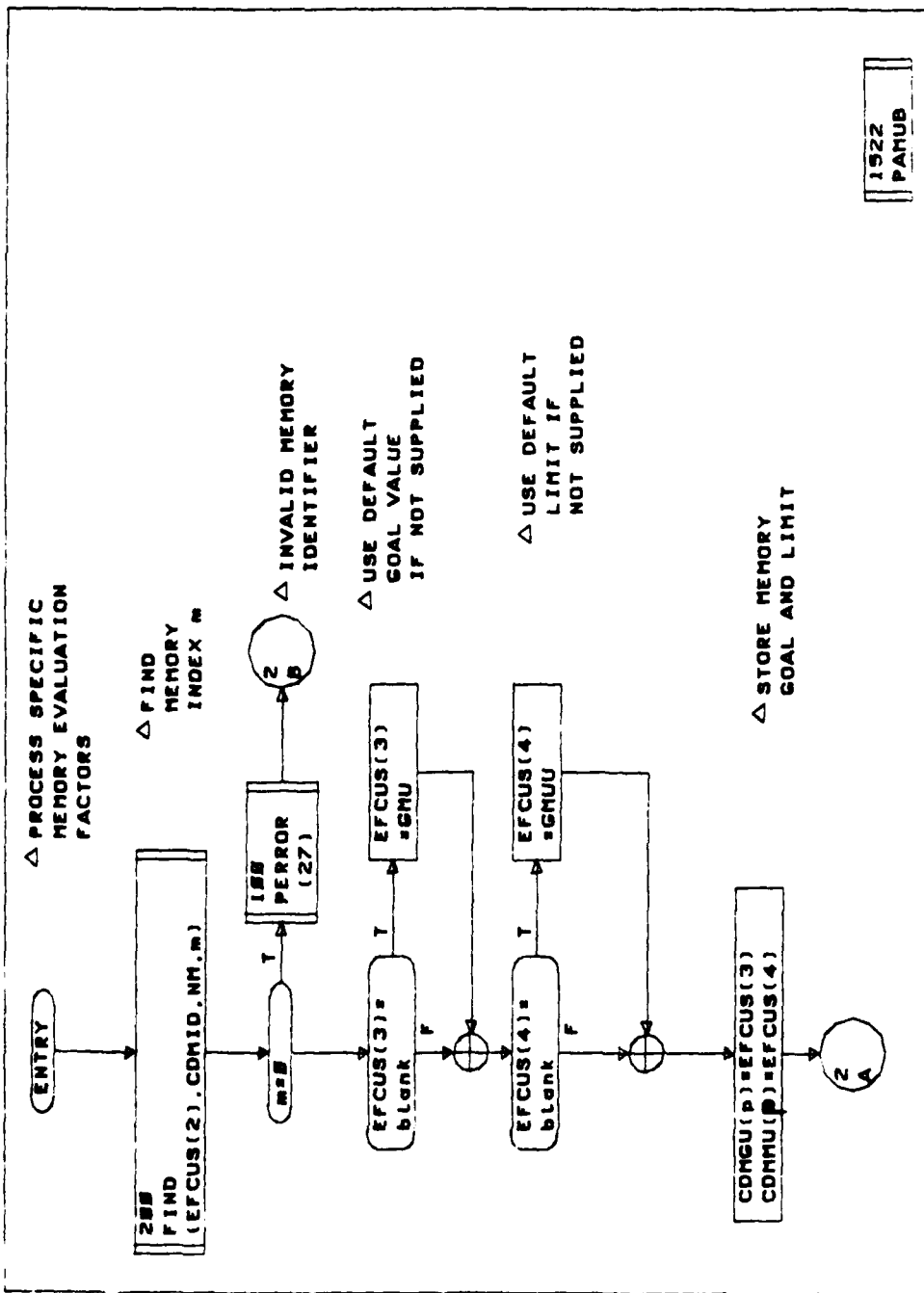
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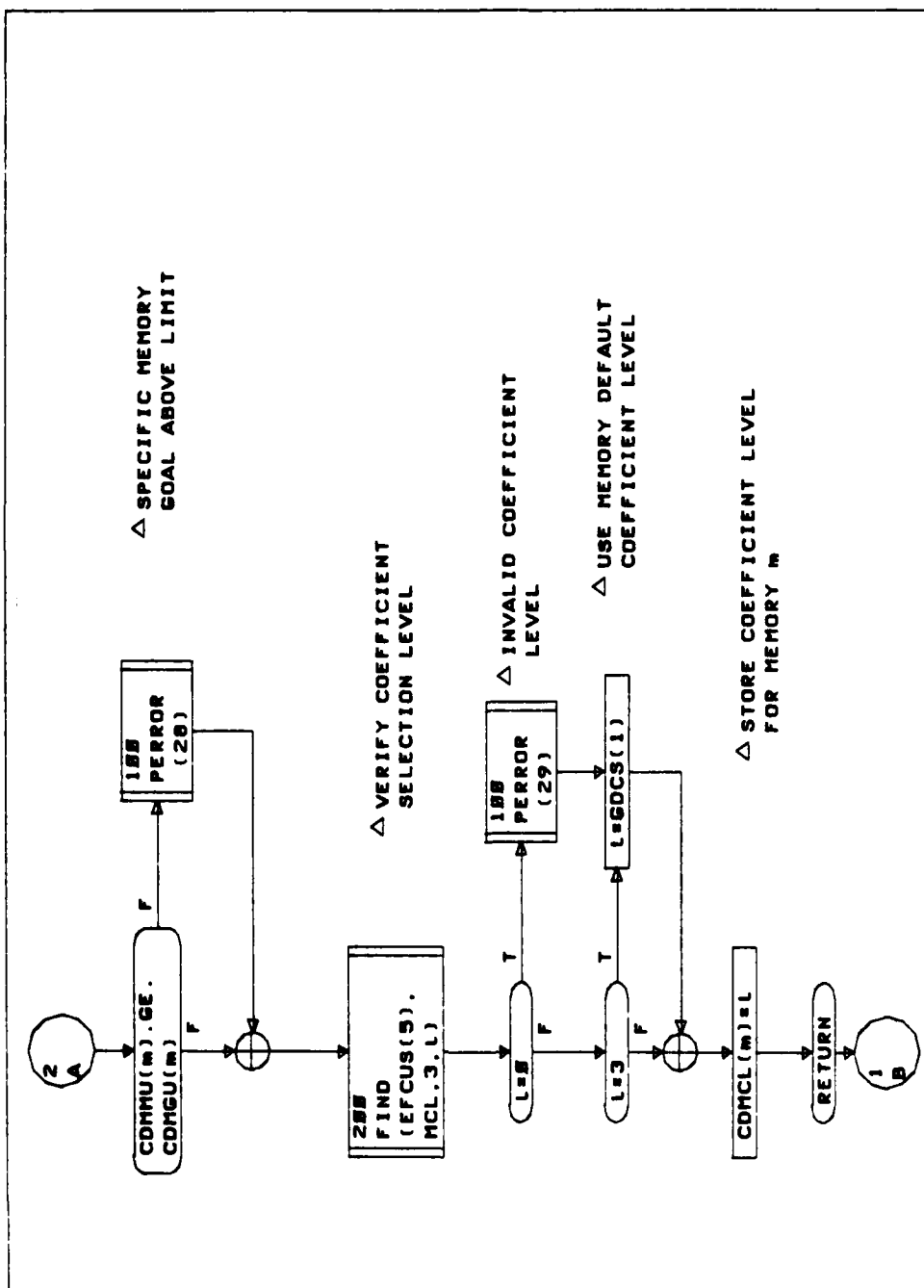


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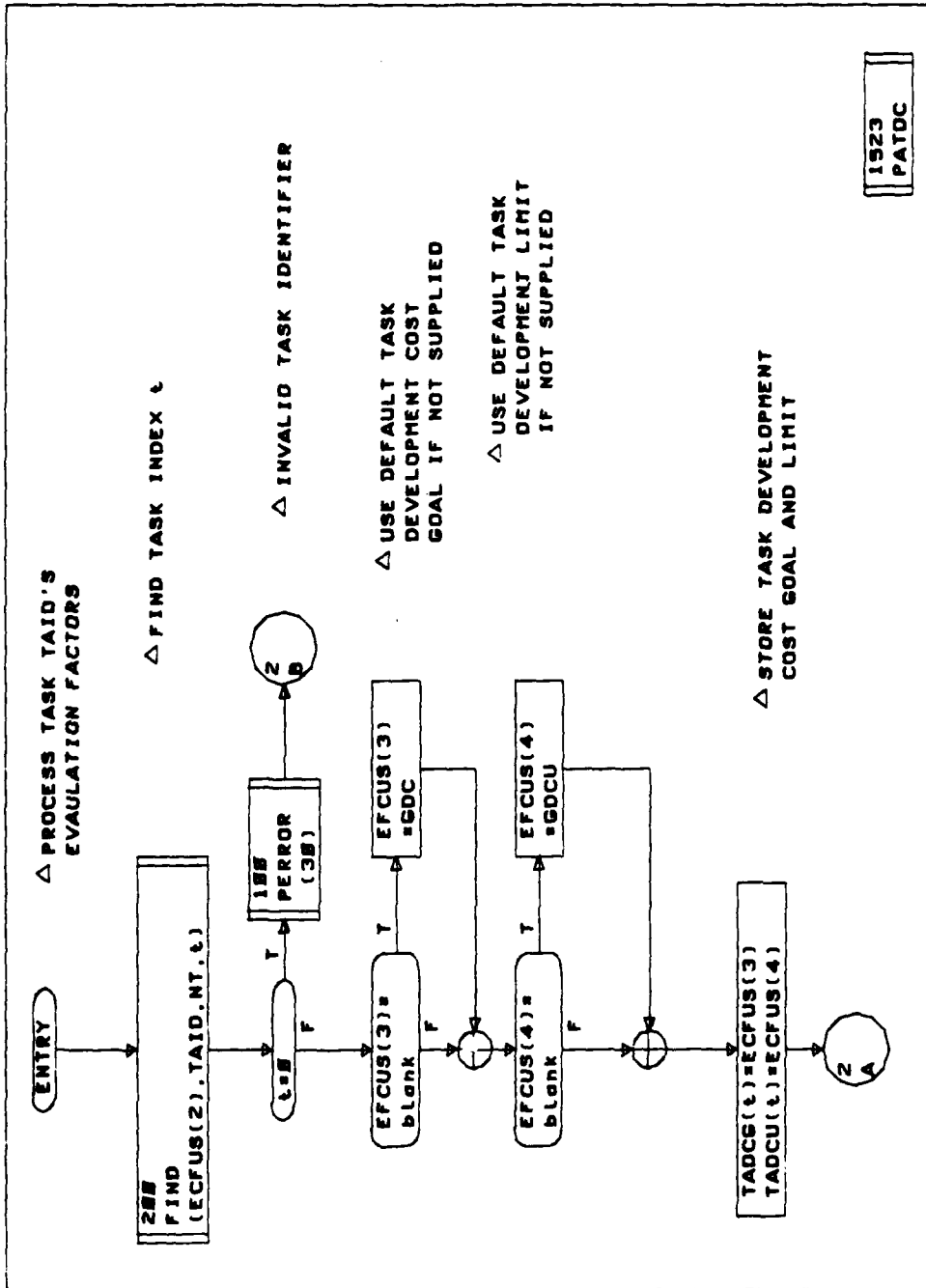


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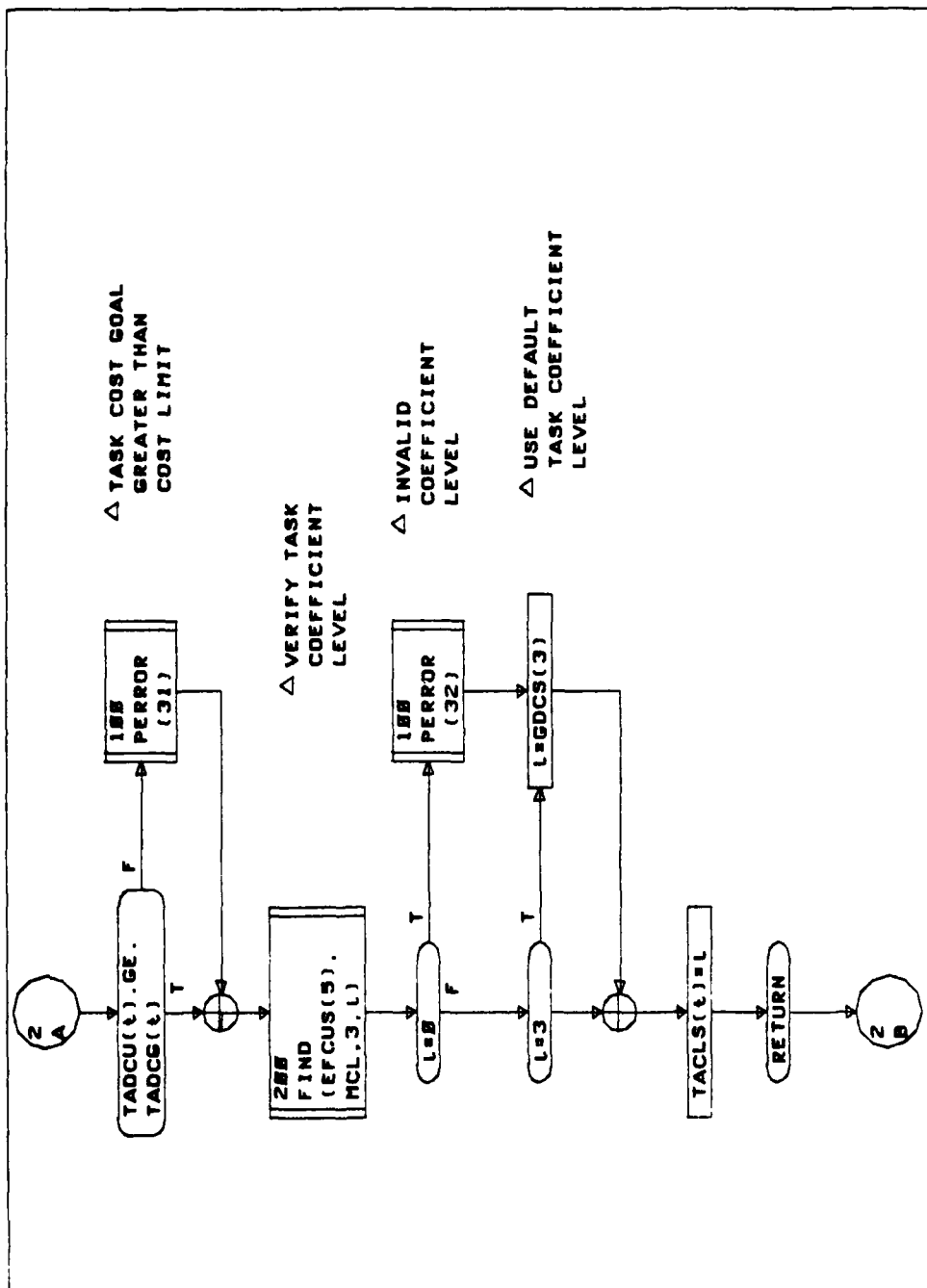




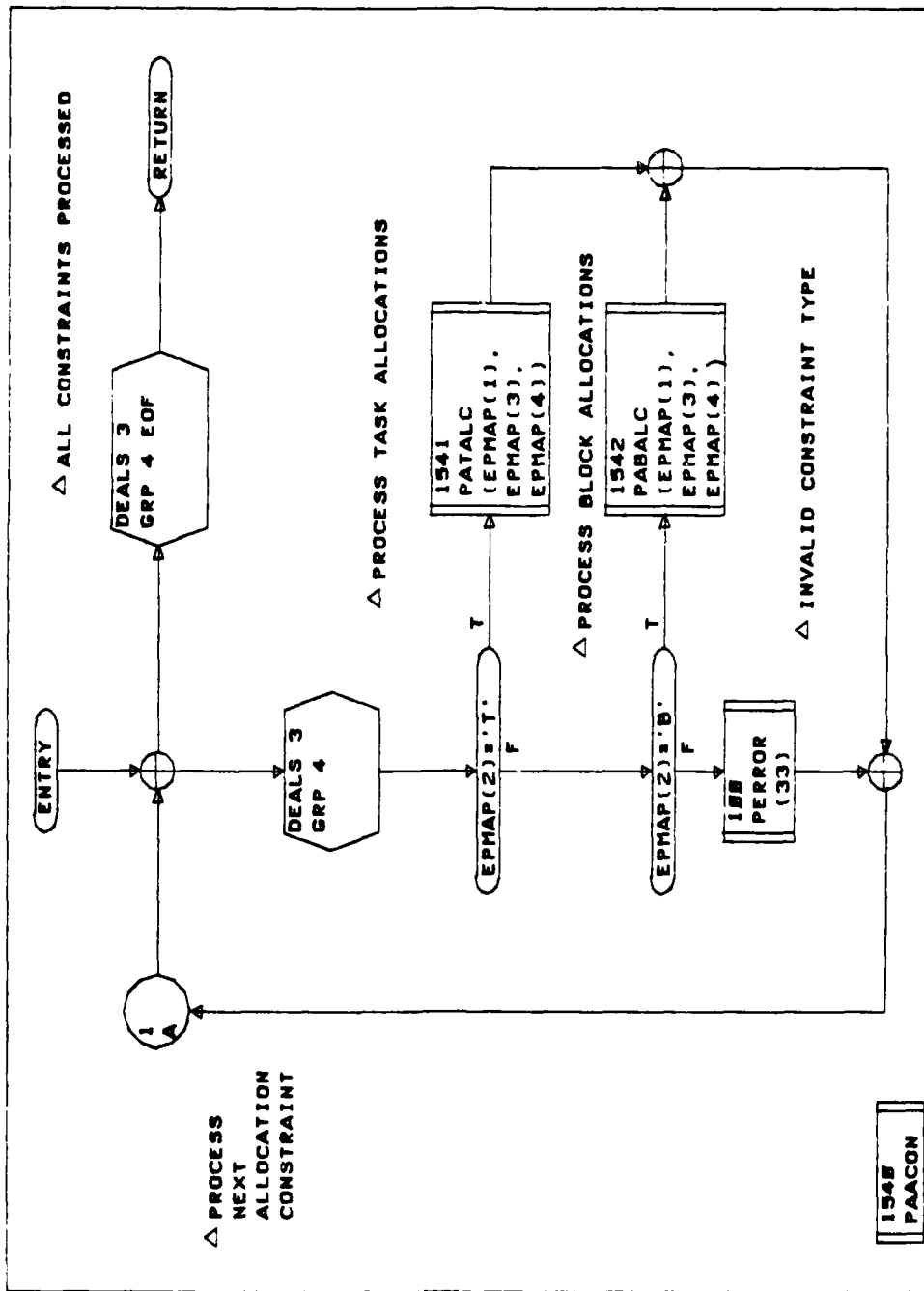
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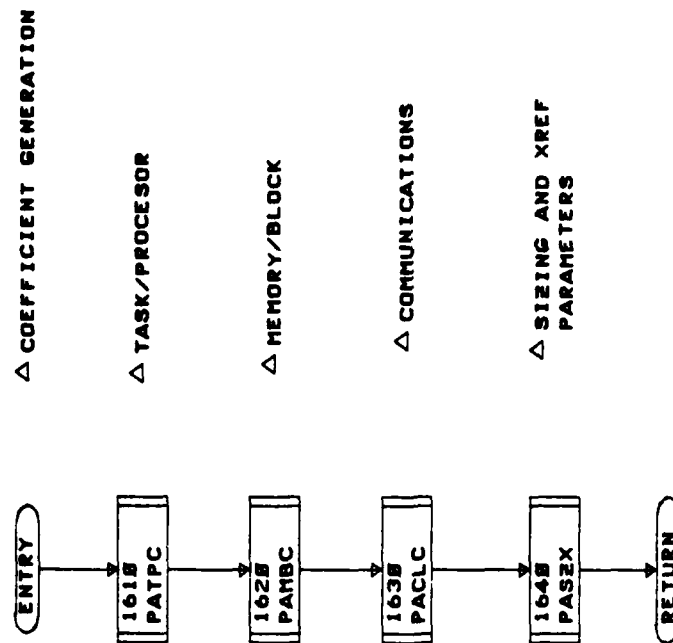


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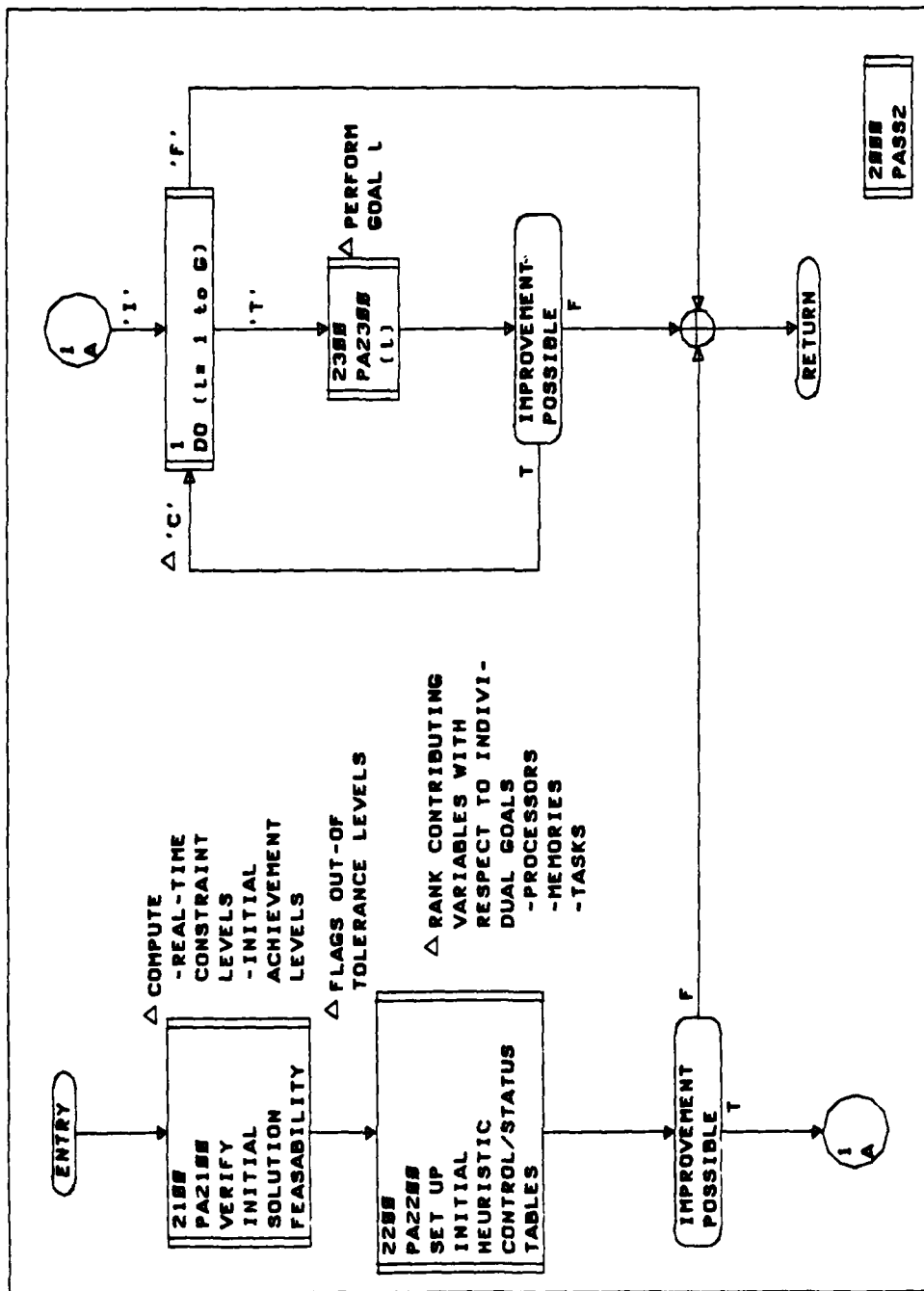


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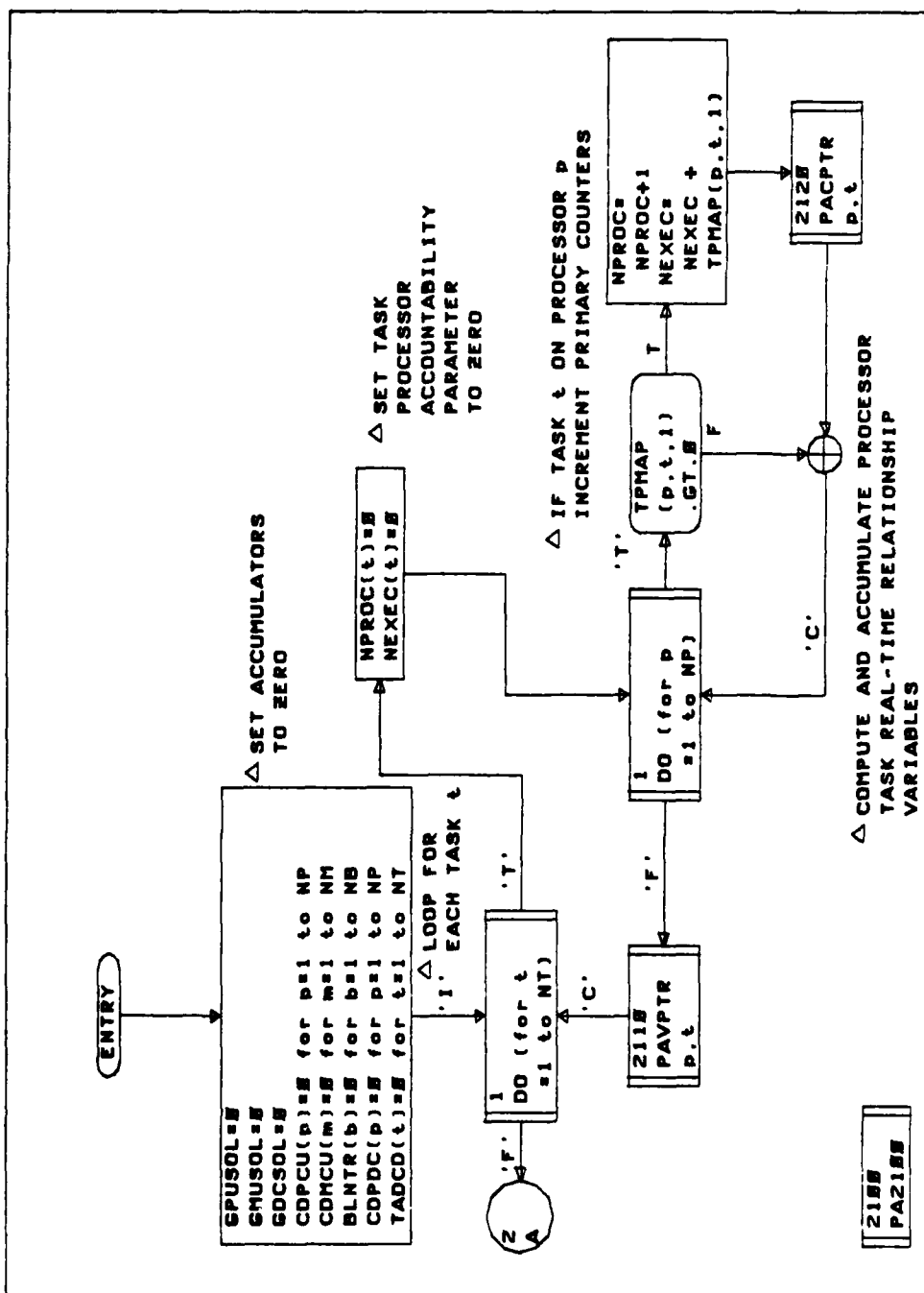
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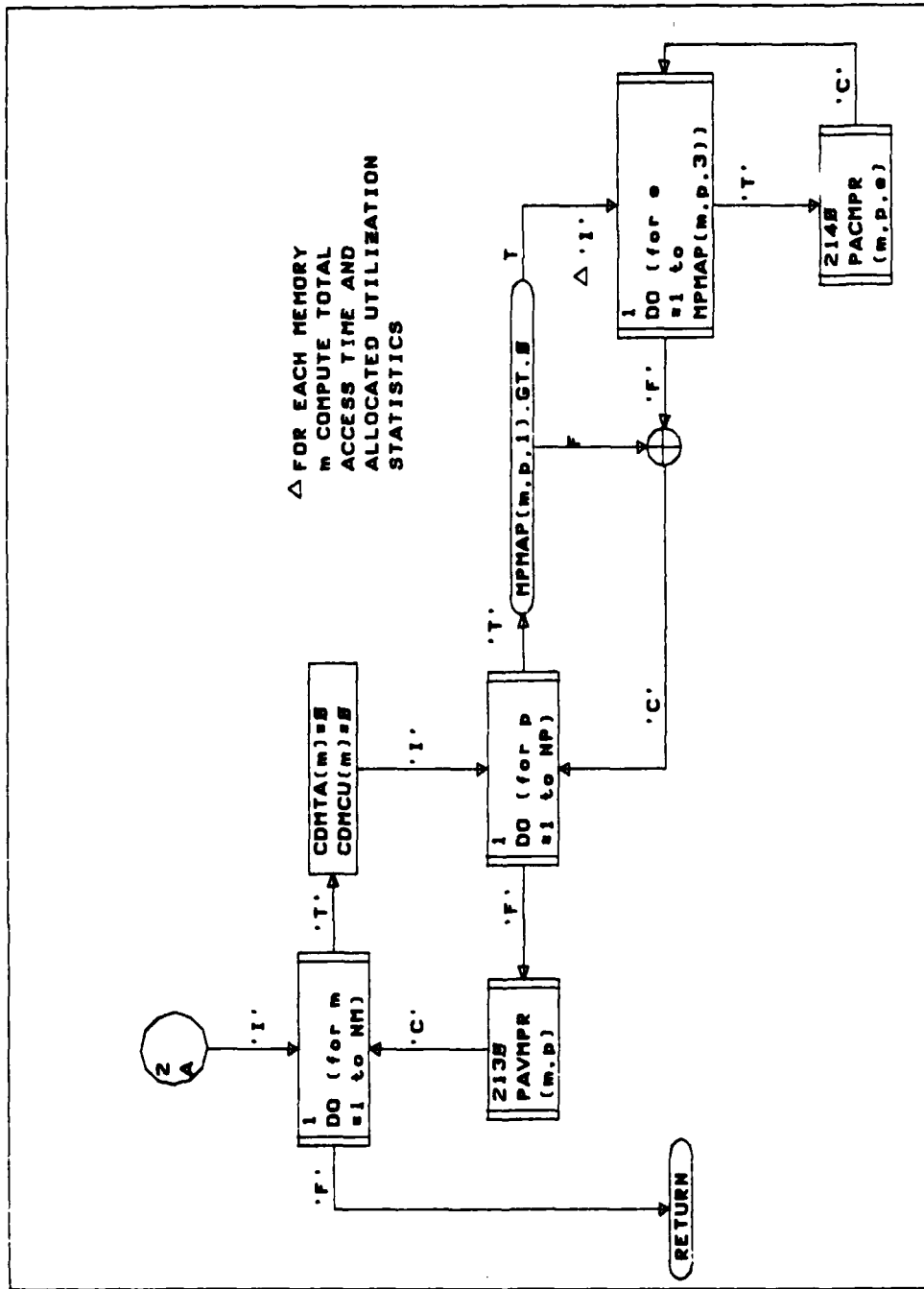


2000
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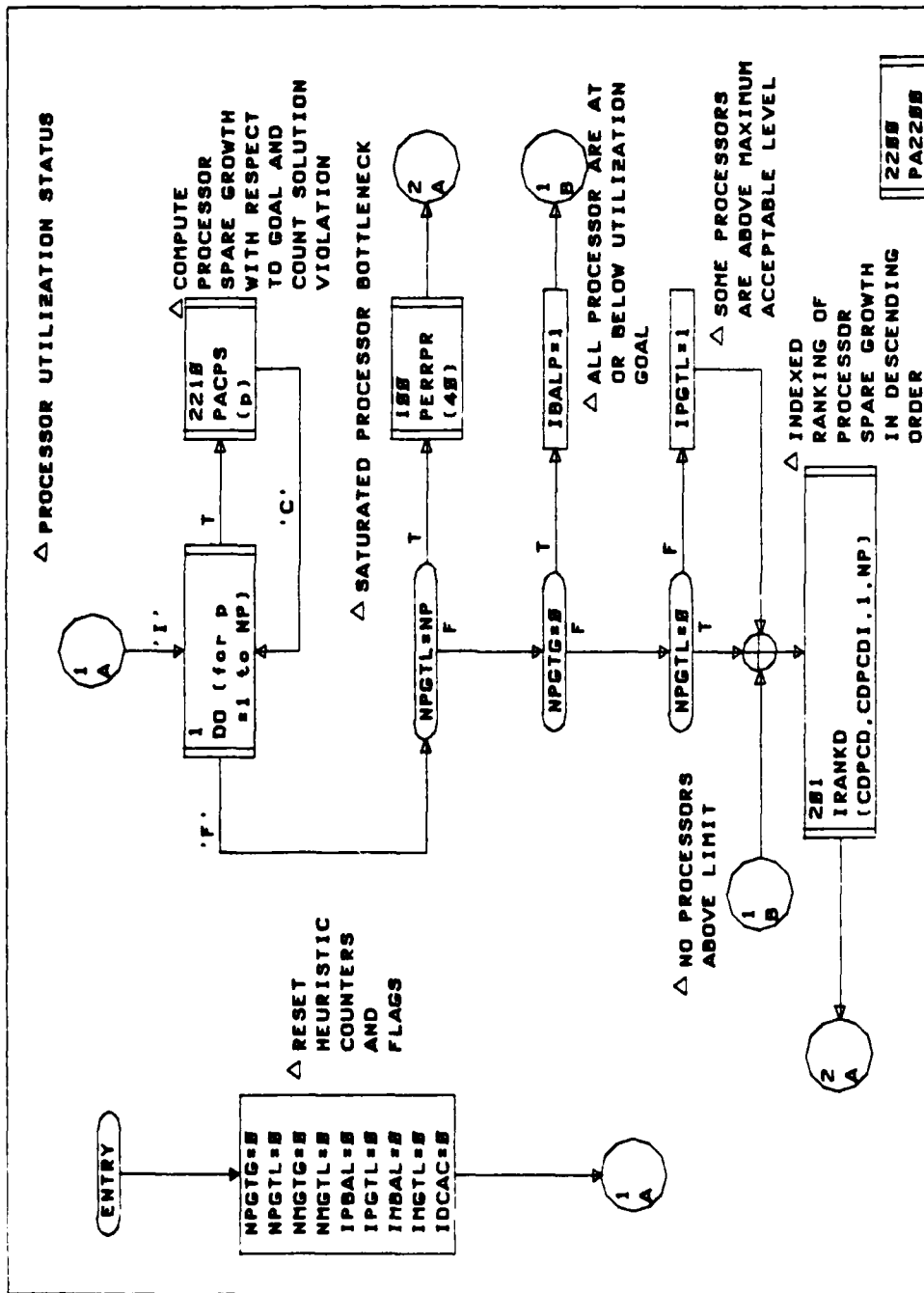
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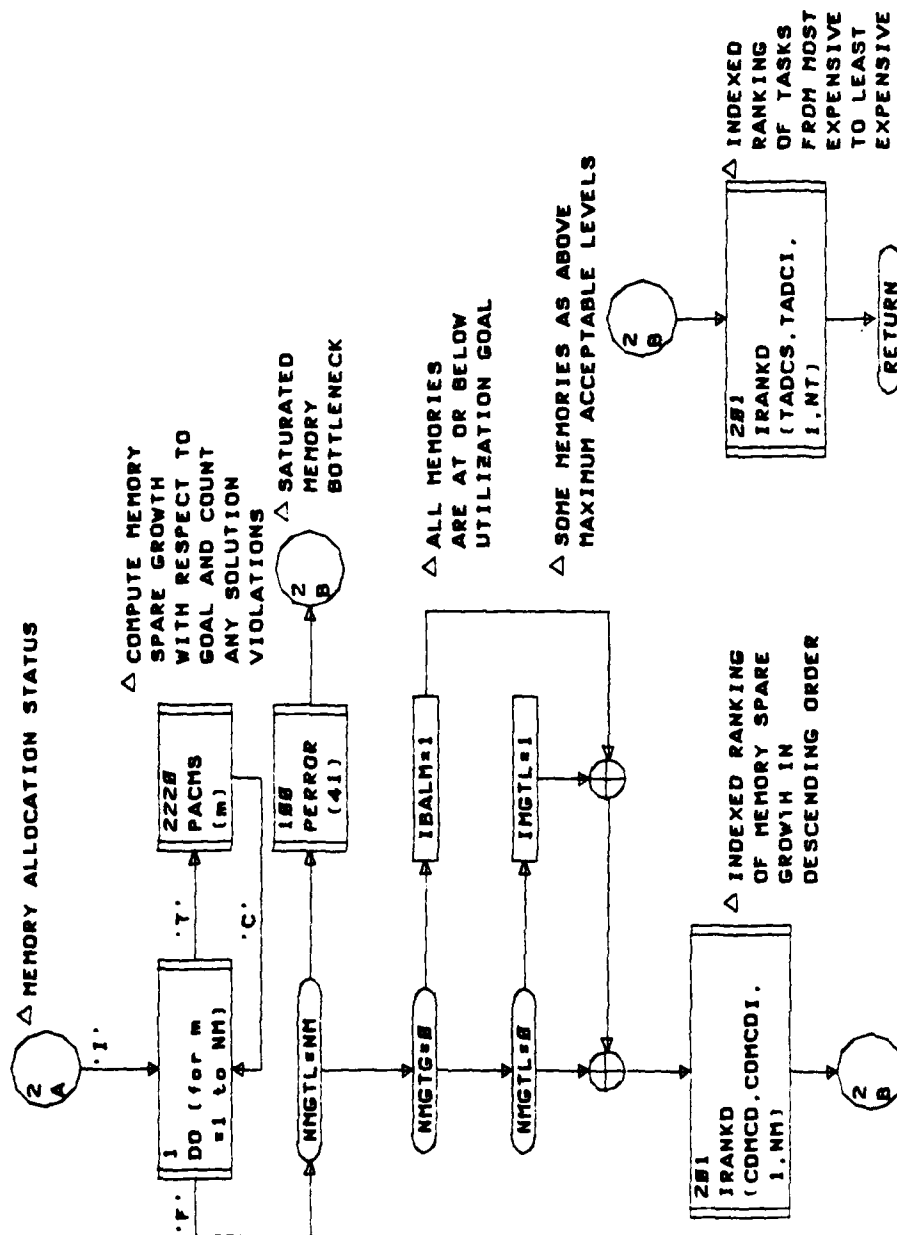


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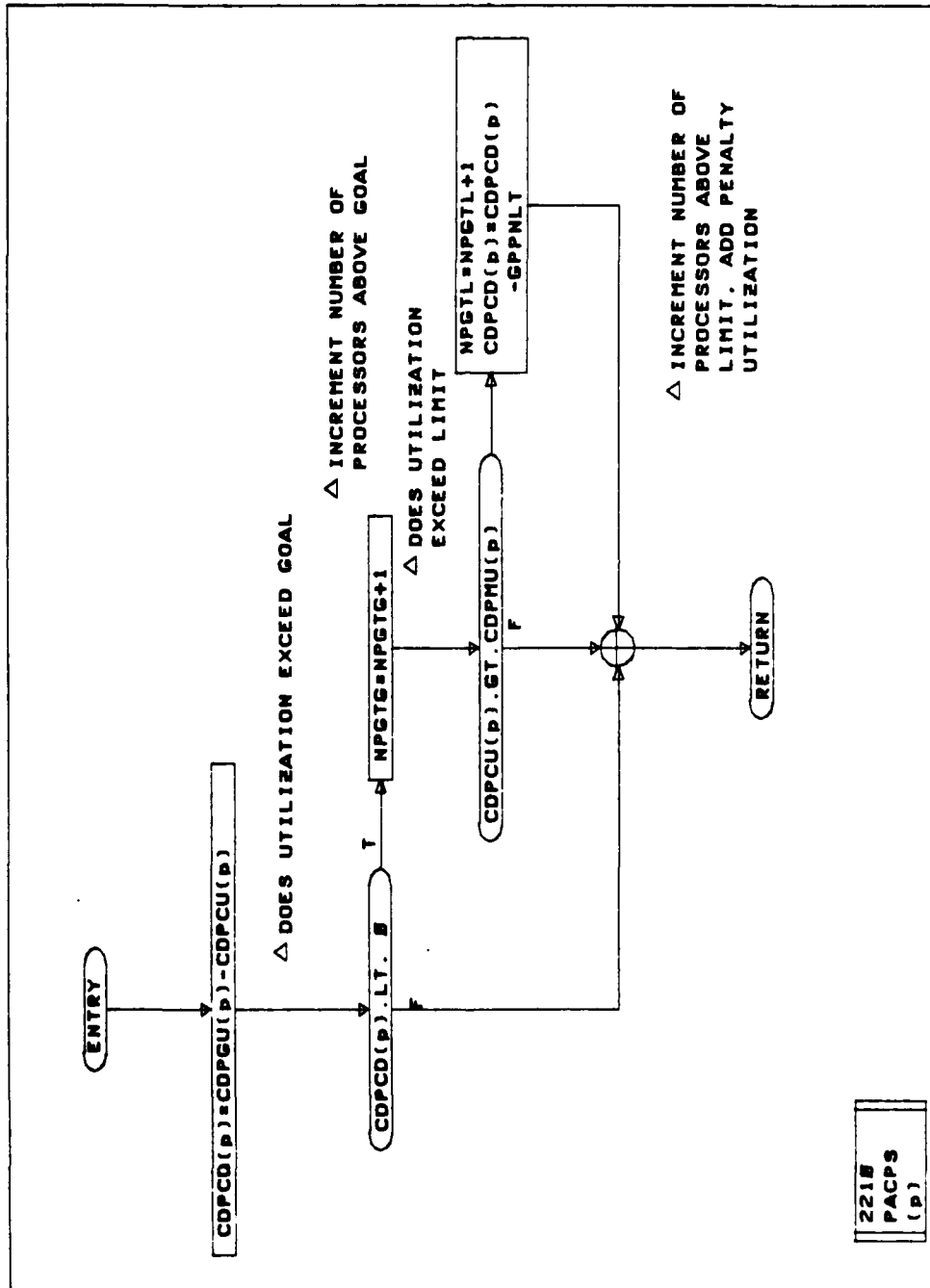


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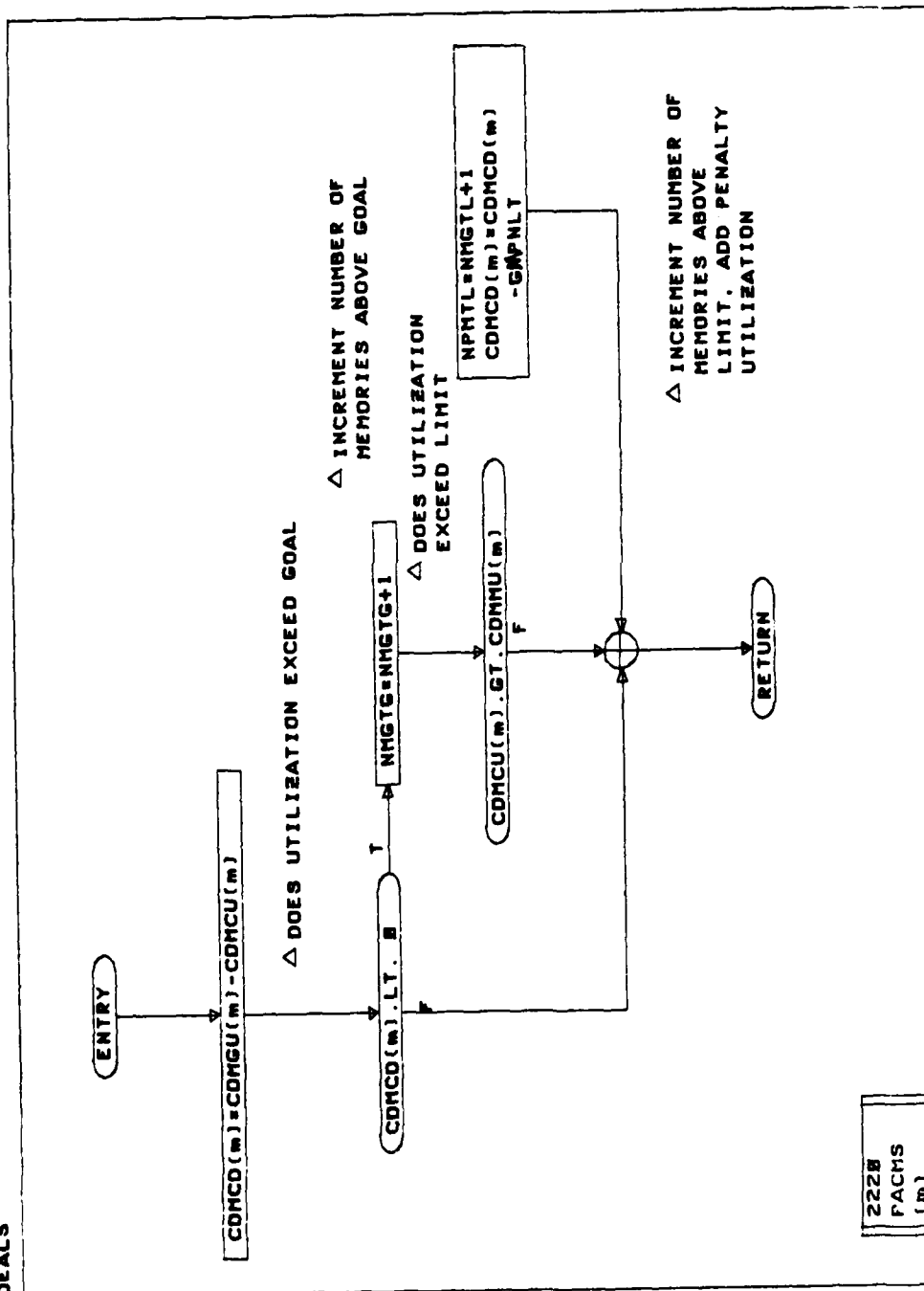


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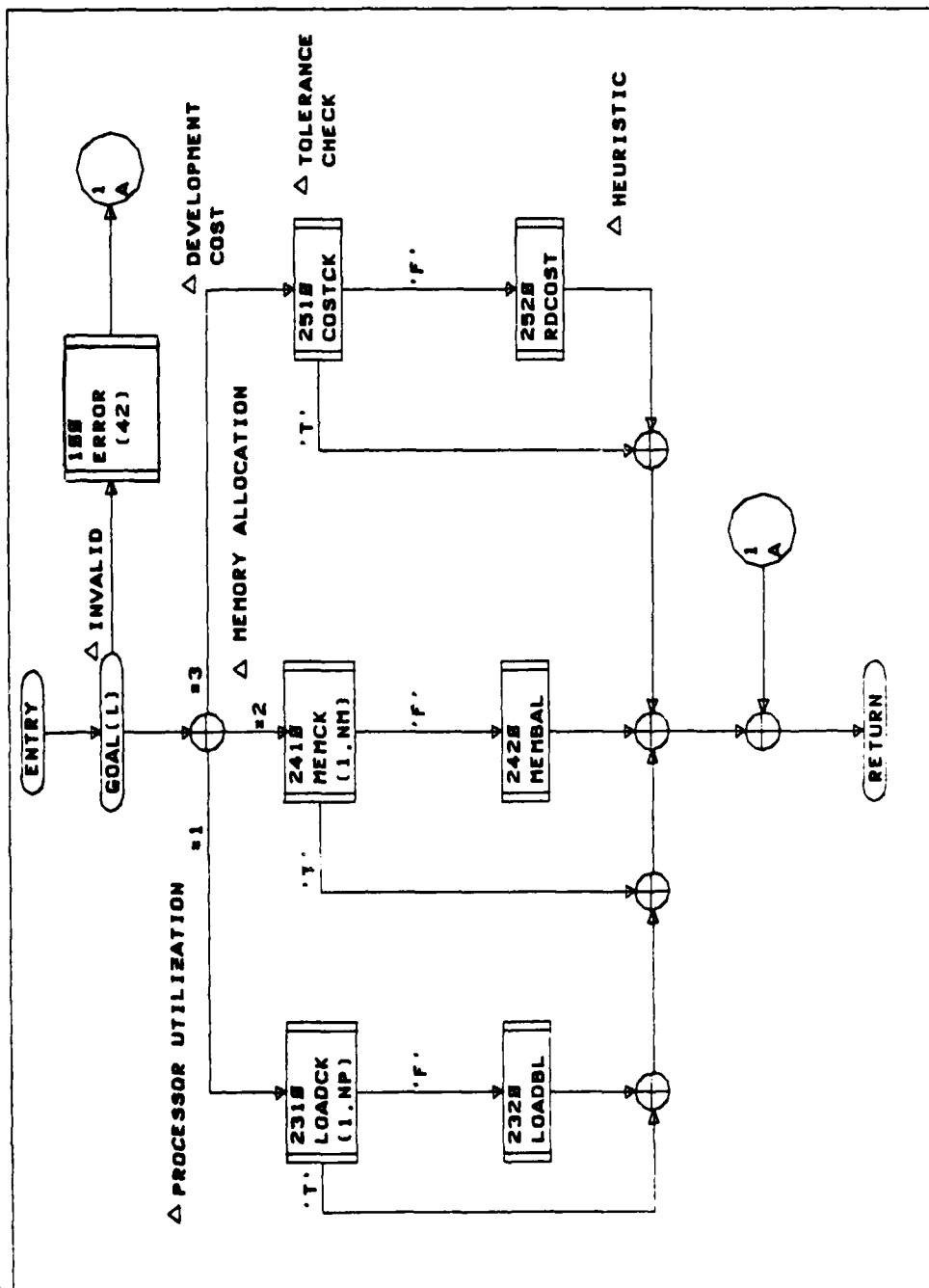
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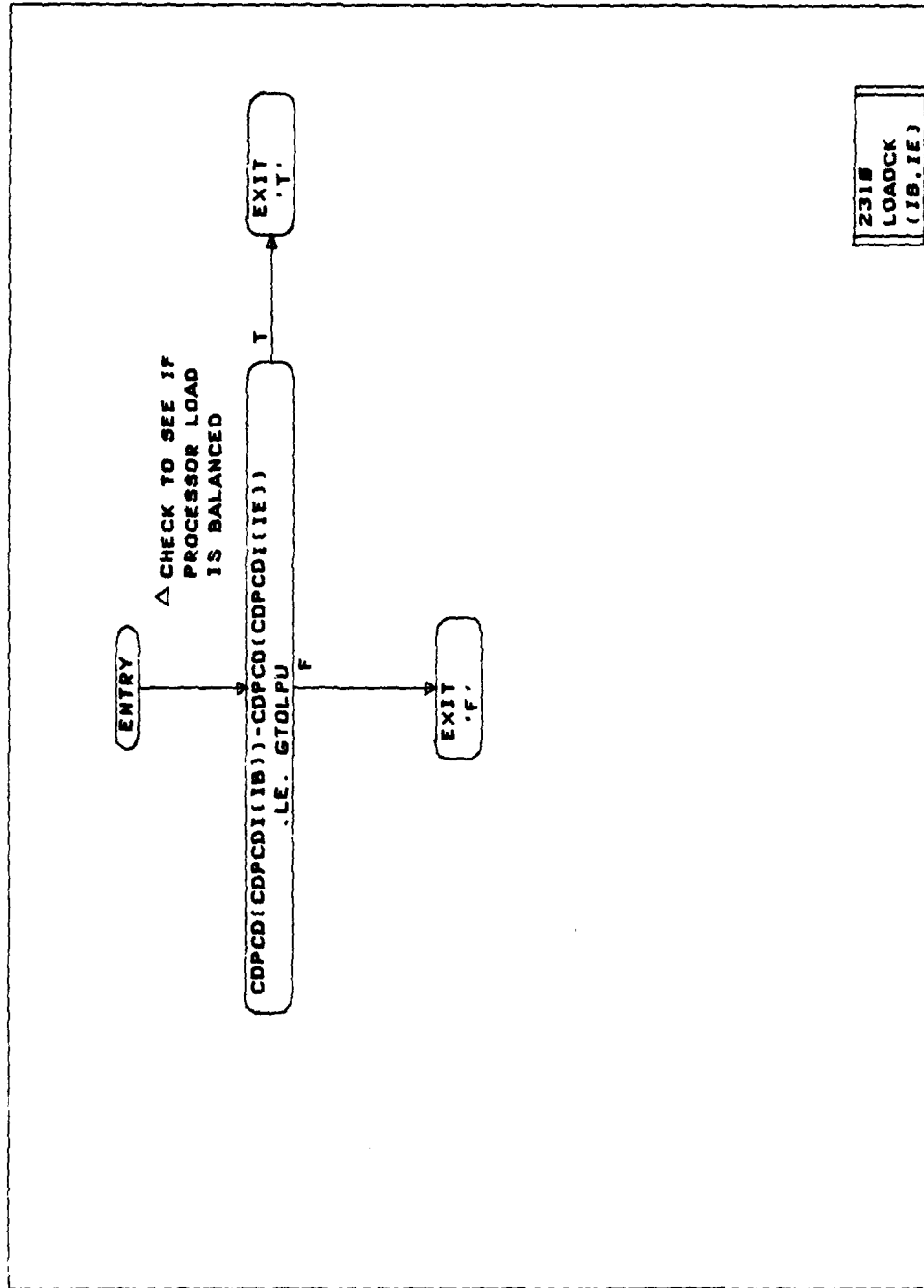


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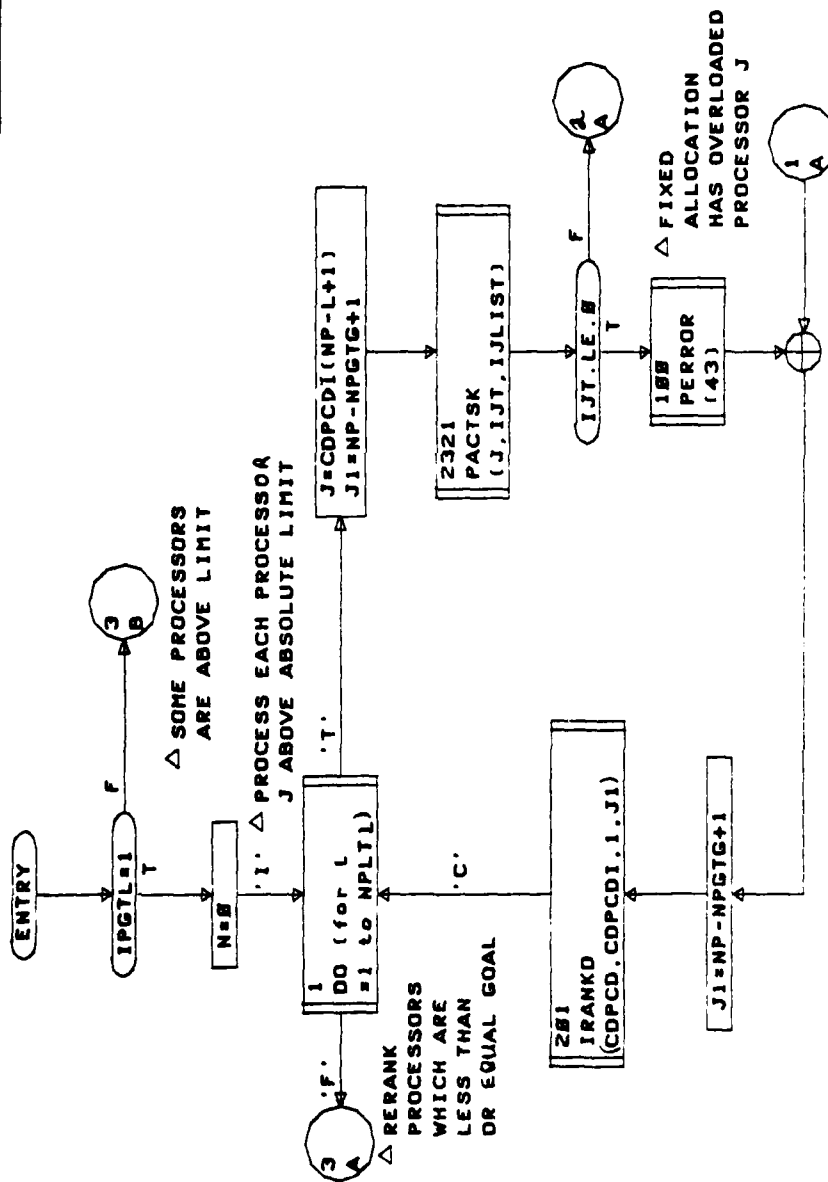
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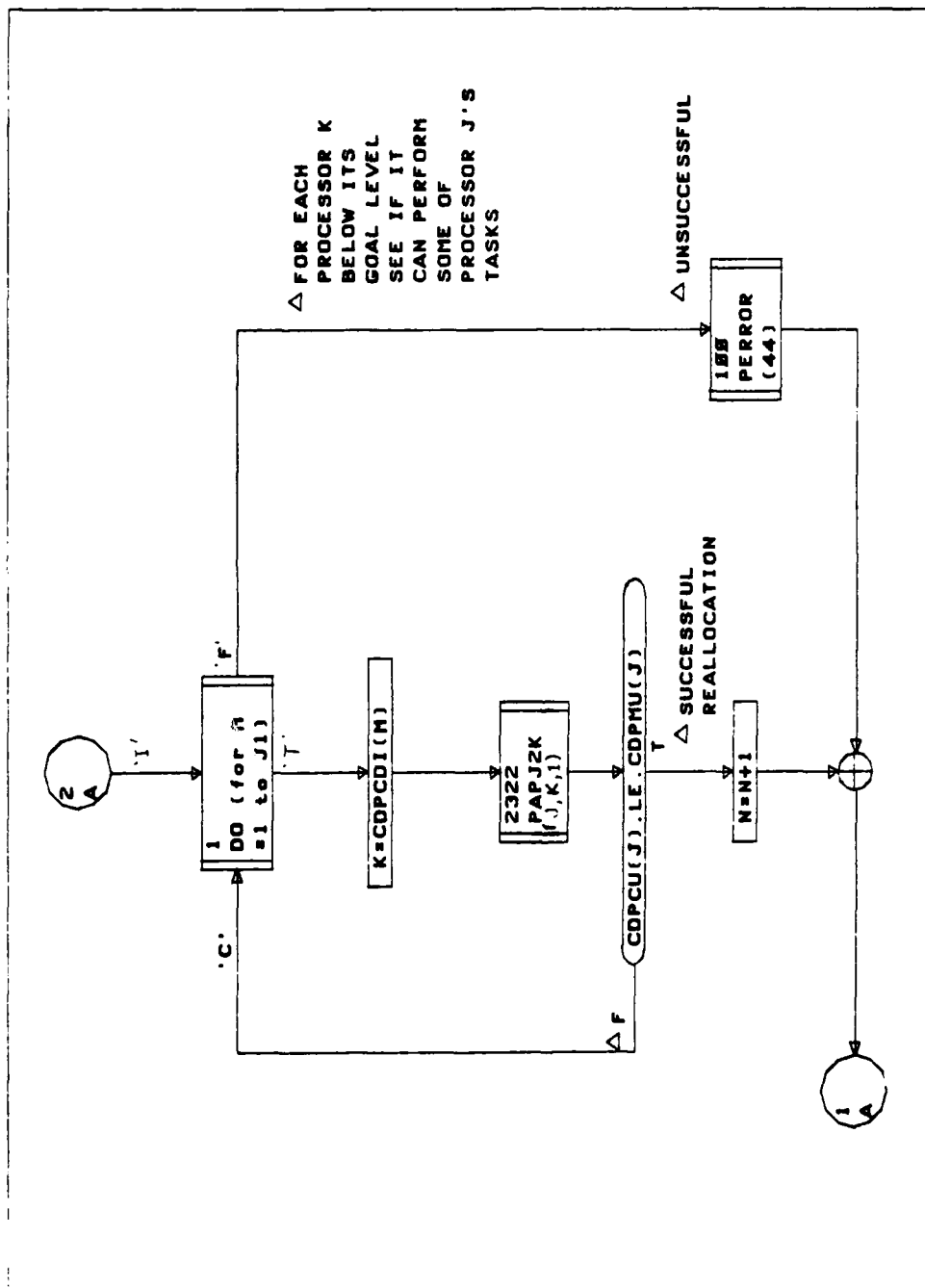


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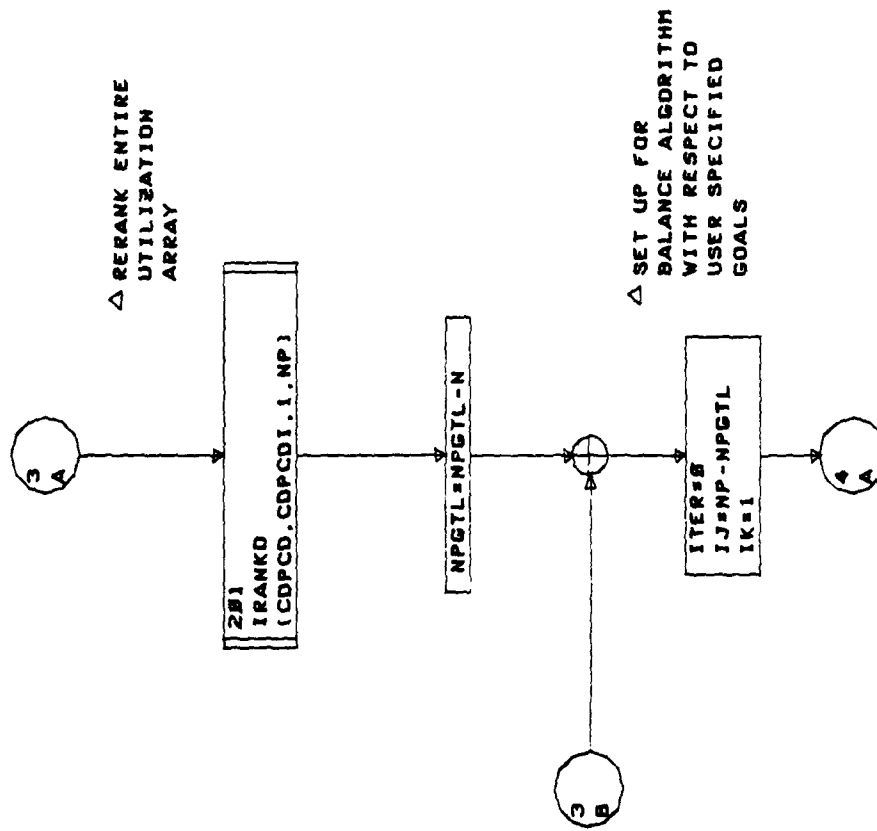


ISSUE DATE 28-NOV-79 ID DEALS SEC PPD-2318 PAGE 1

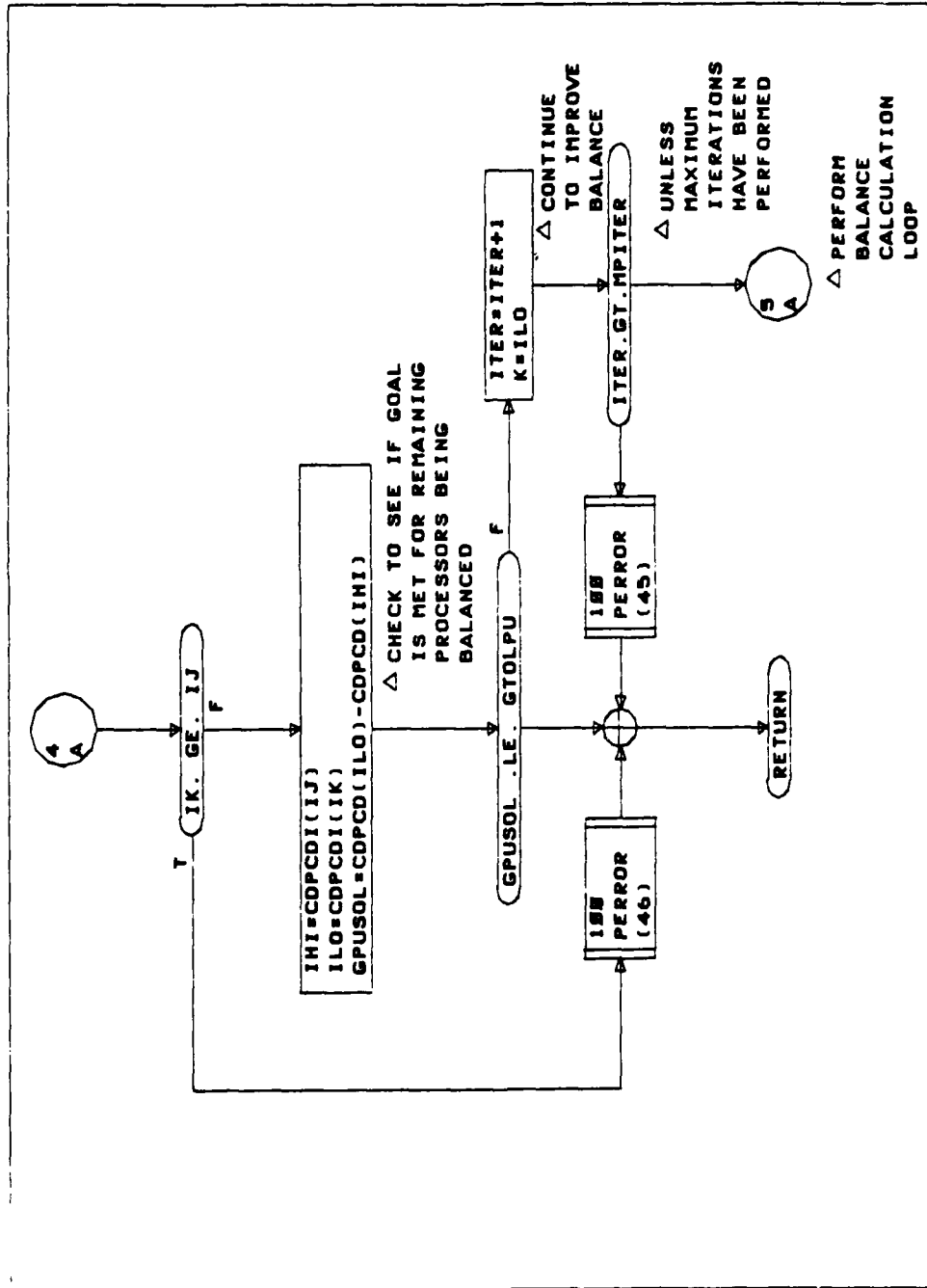




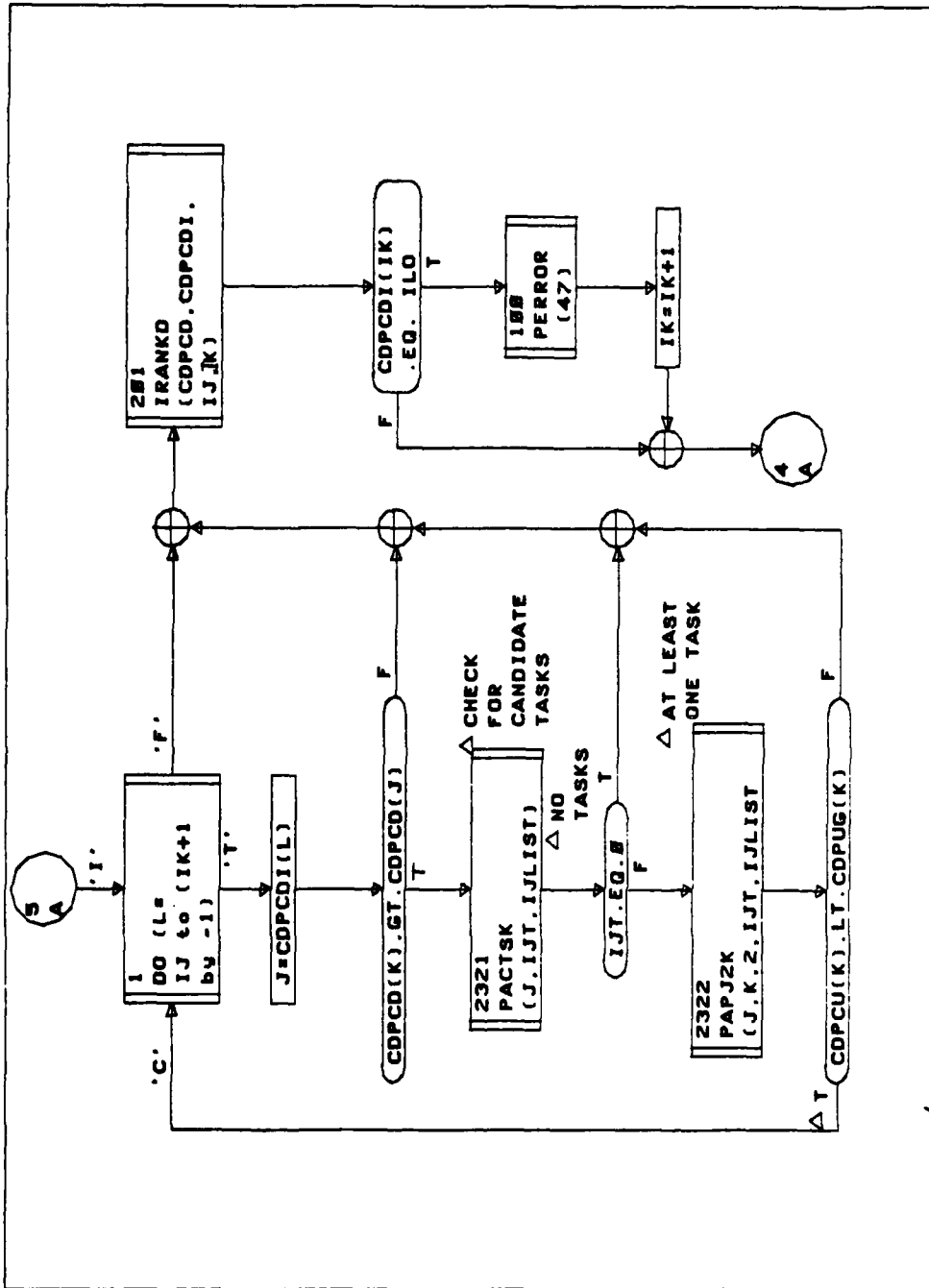
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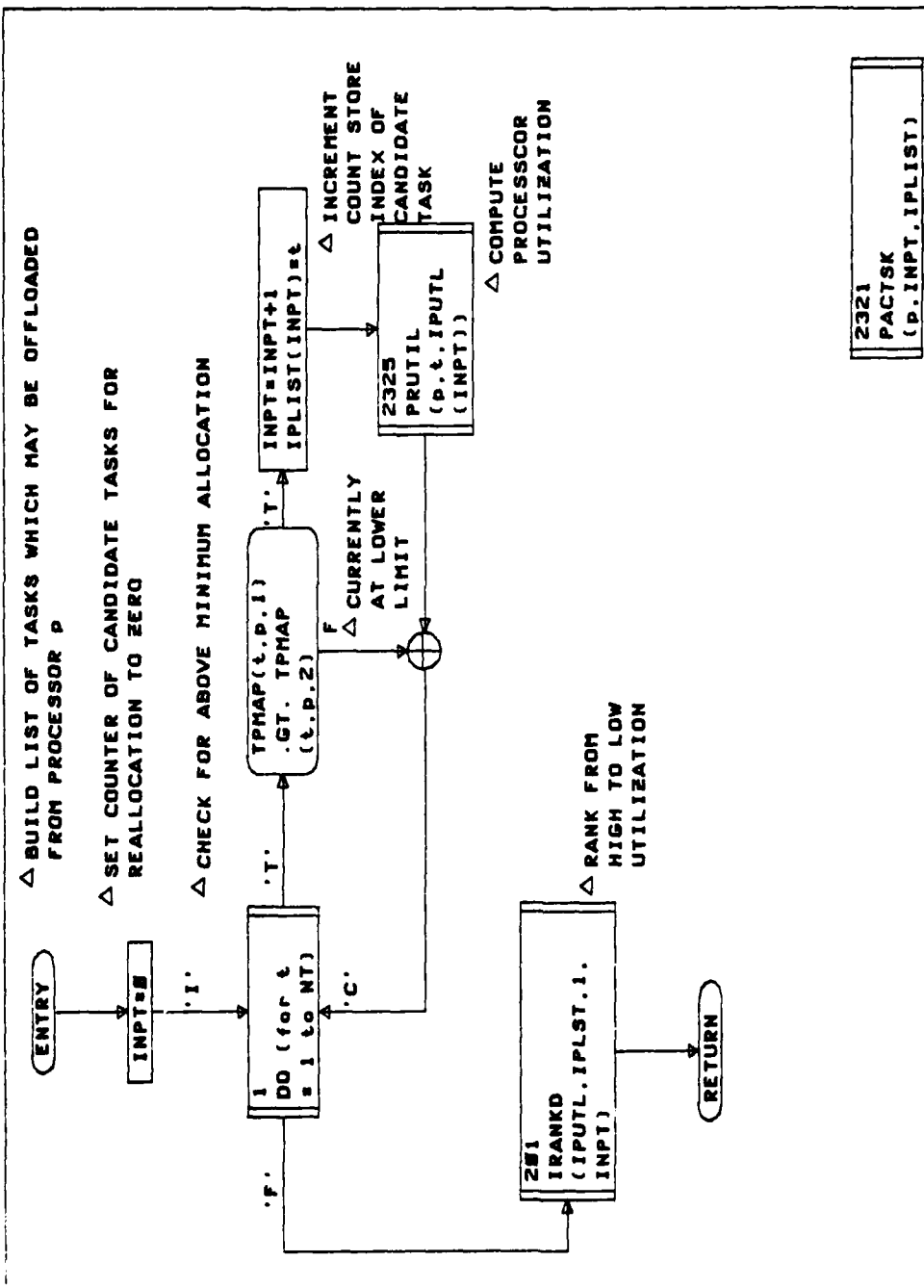
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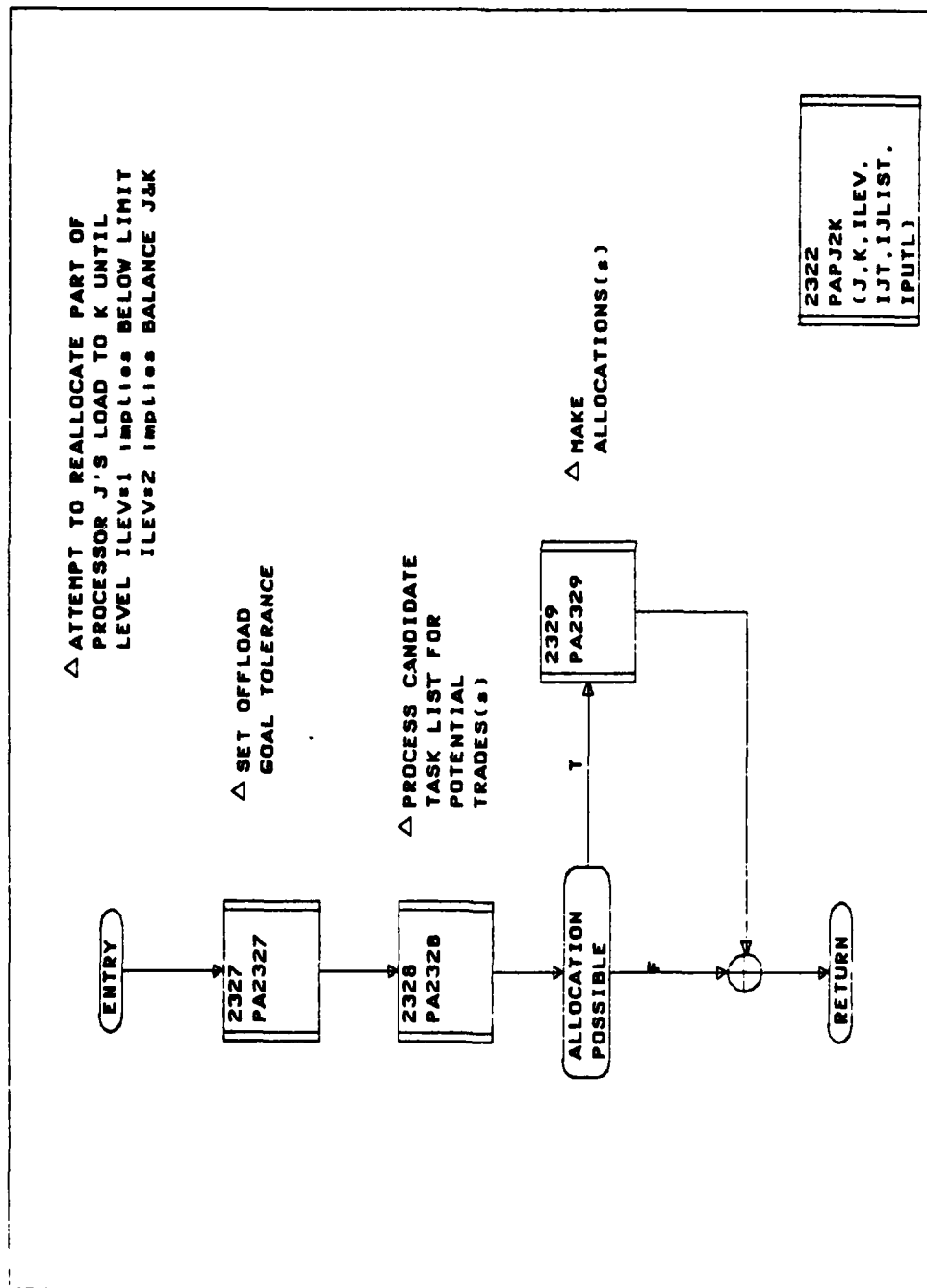


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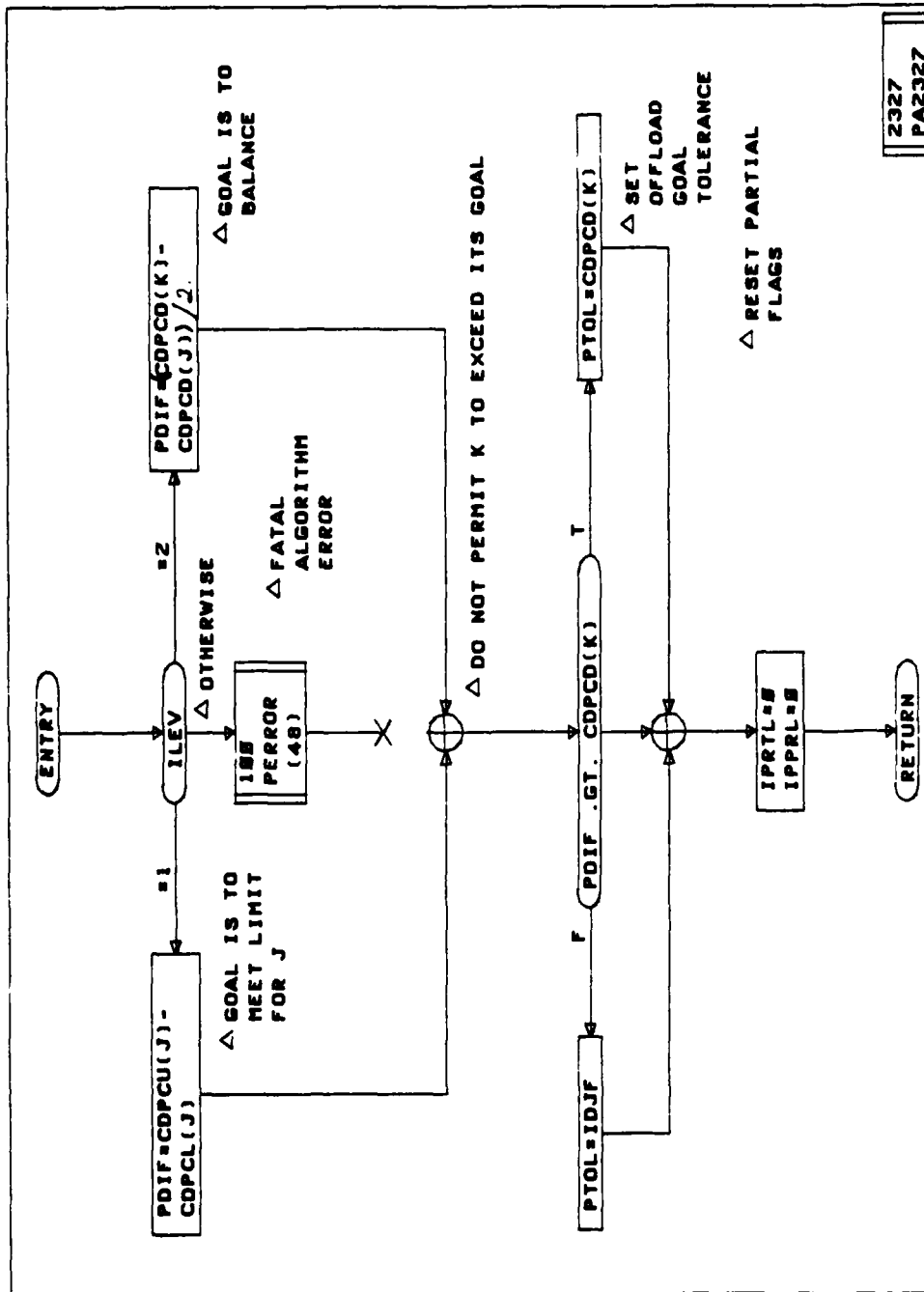


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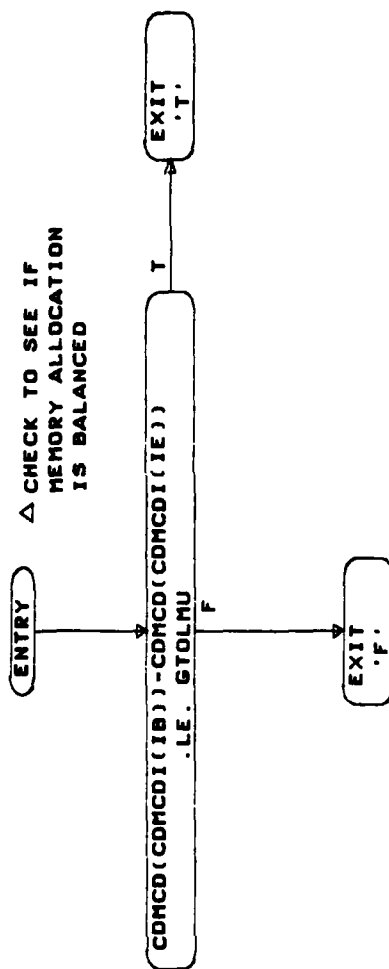


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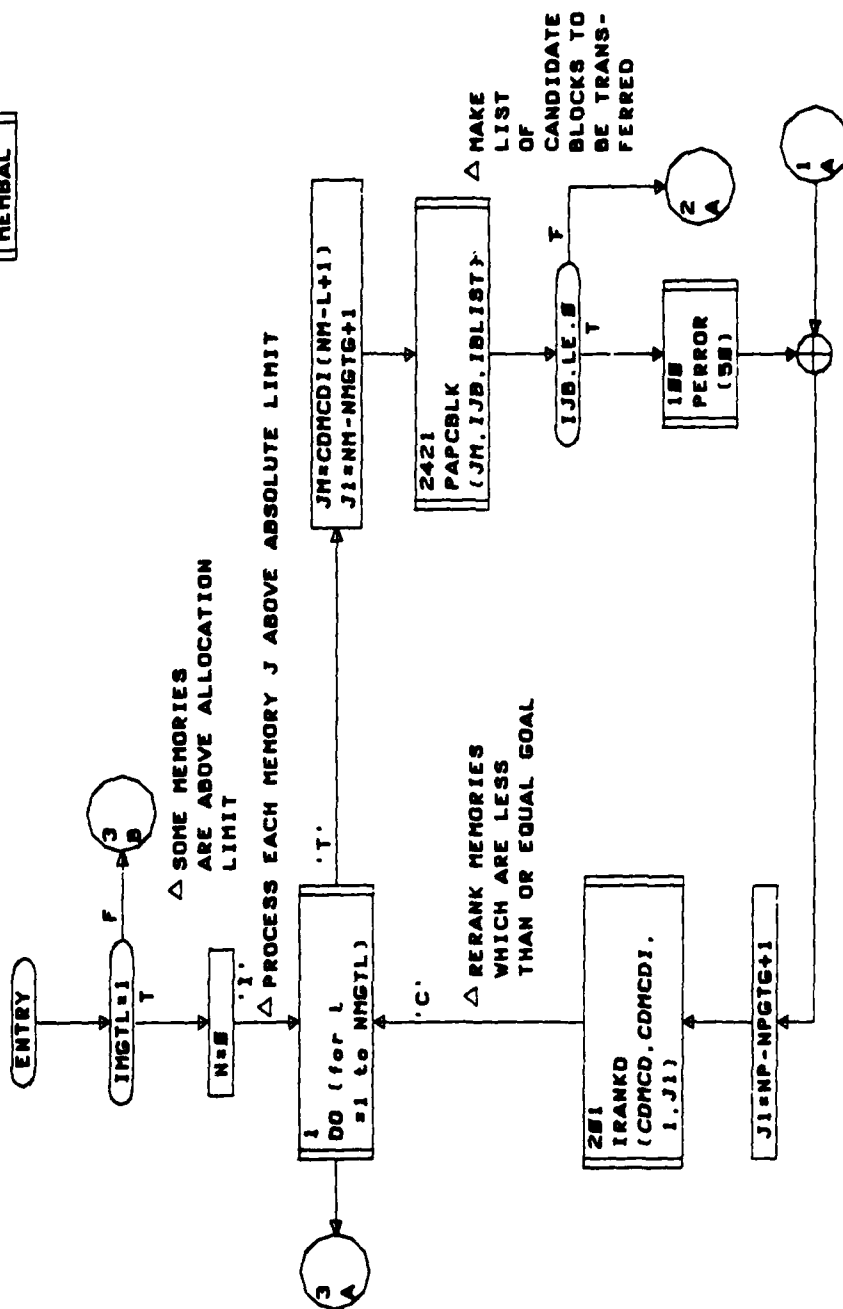
ISSUE DATE 28-NOV-79 10 DEALS SEC PPD-2327 PAGE 1

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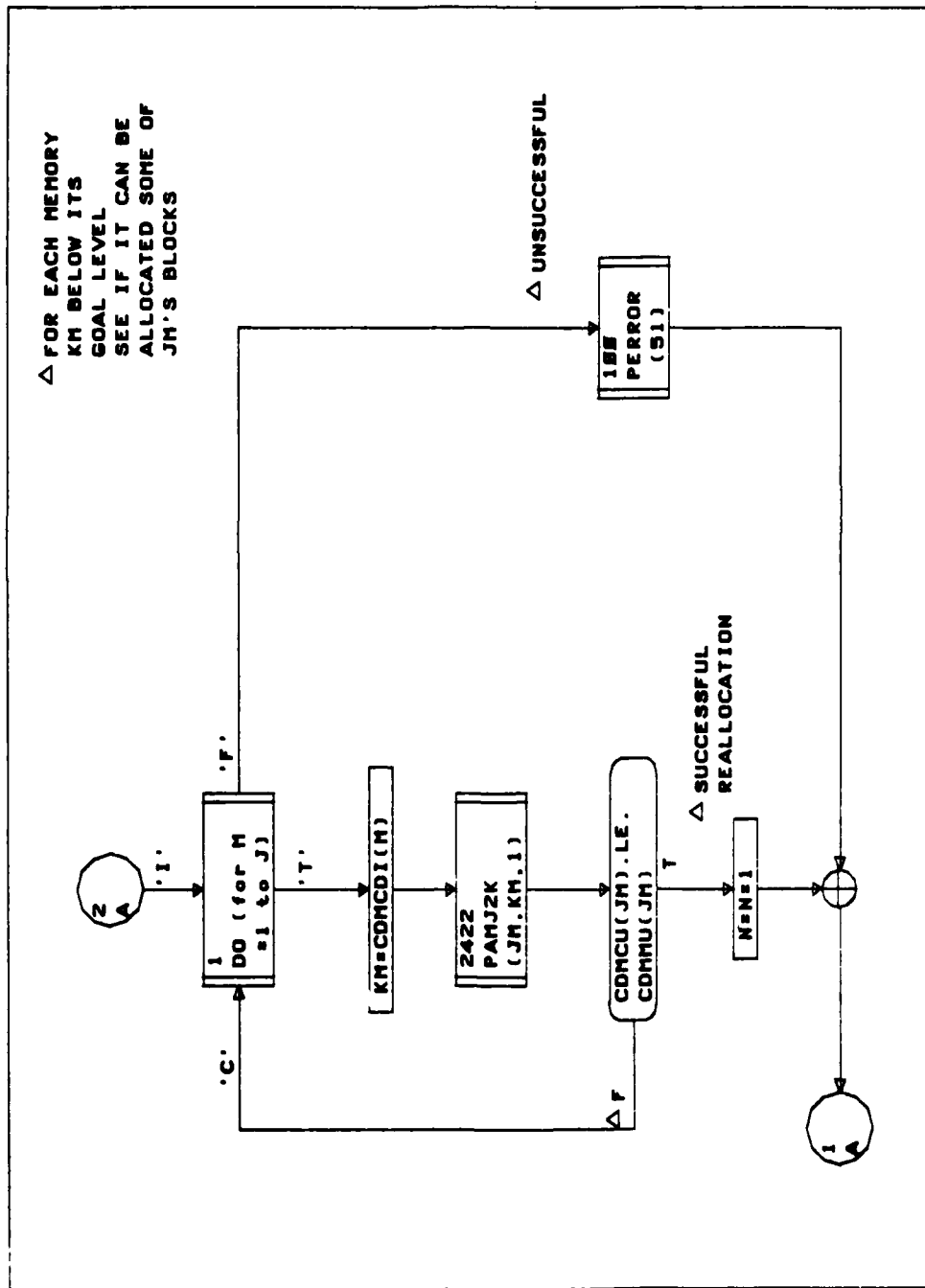


241B
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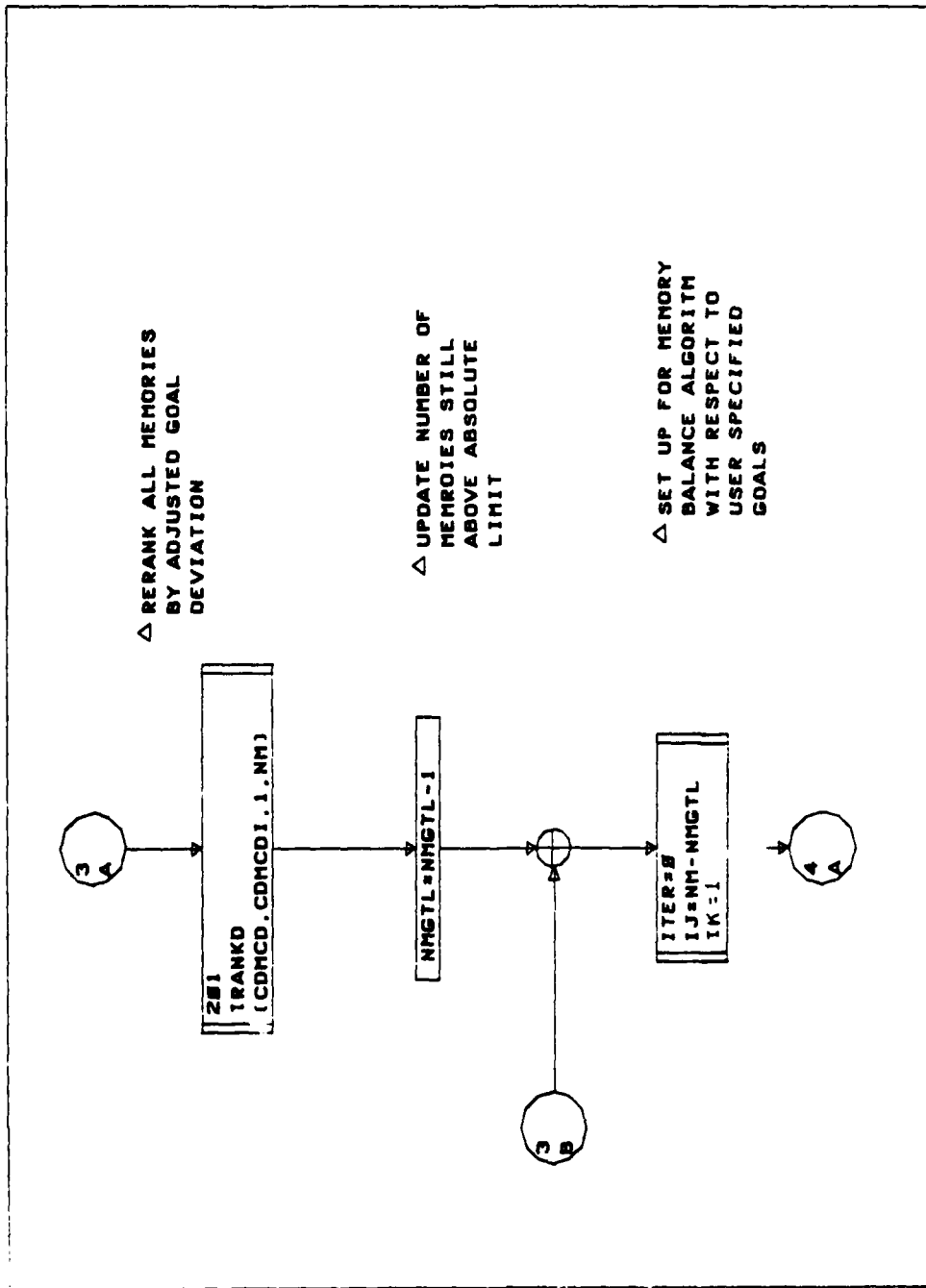
ISSUE DATE 28-NOV-79 ID DEALS SEC PPD-241B PAGE 1



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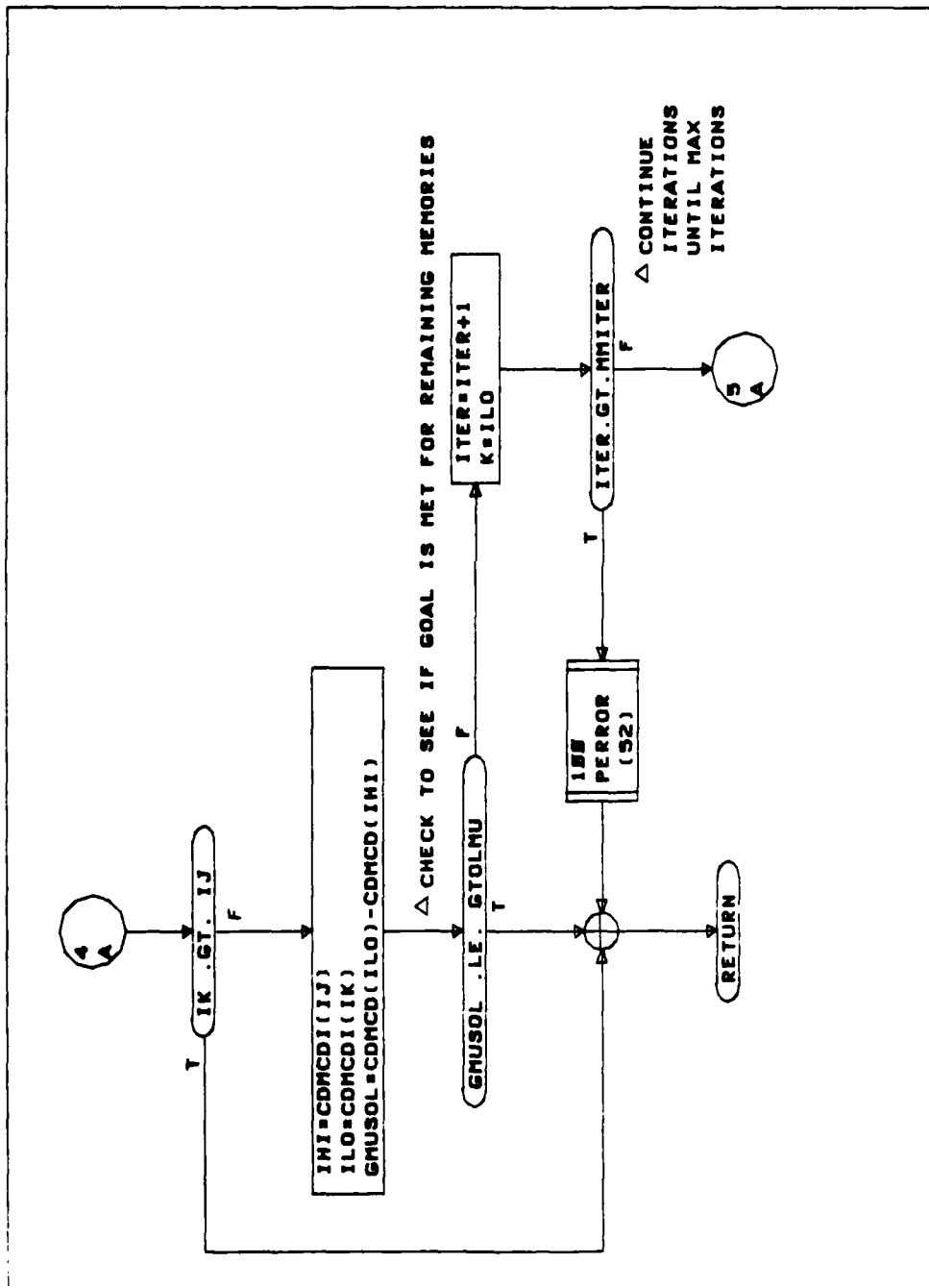


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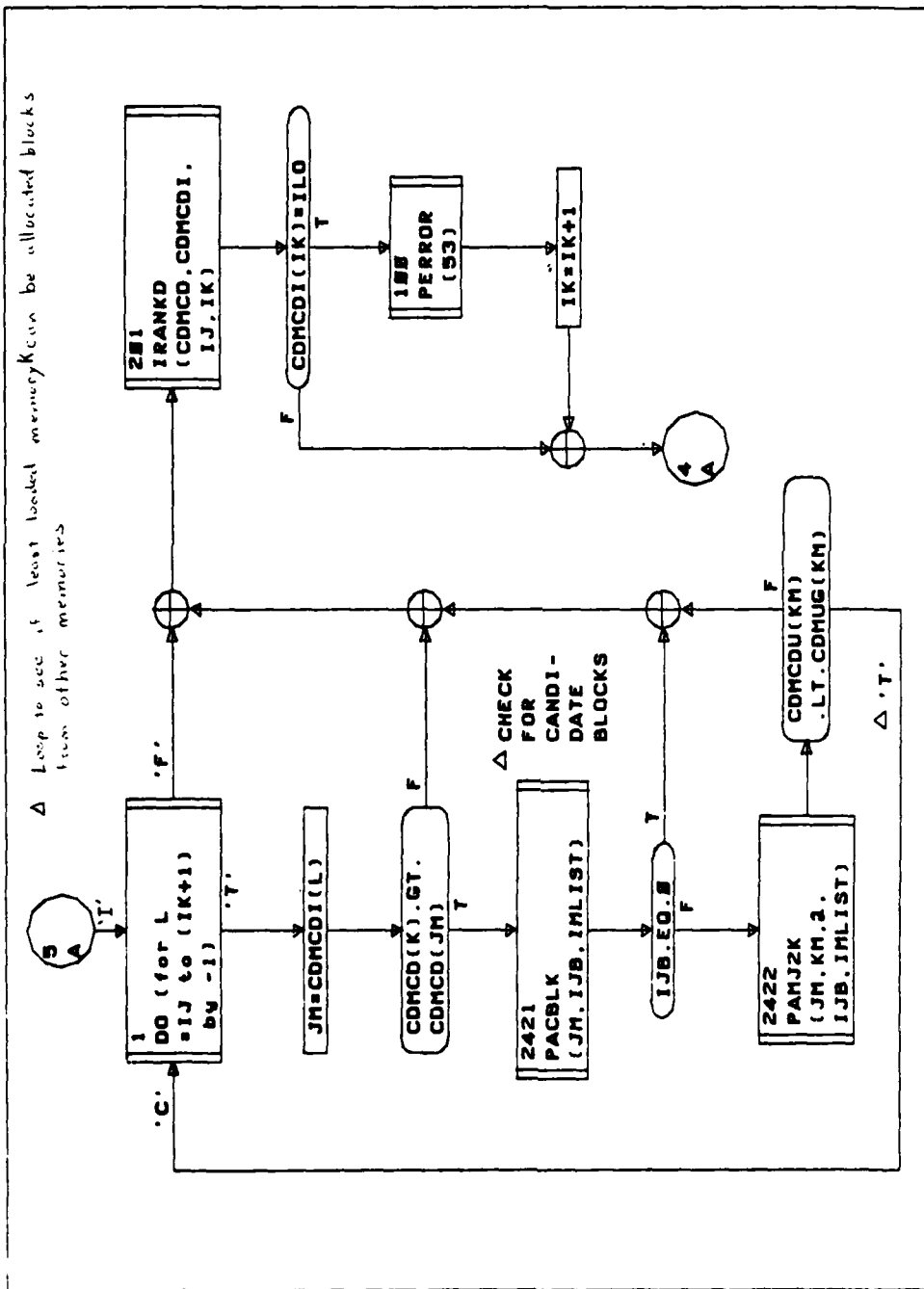


ISSUE DATE 26-NOV-79 ID DEALS SEC PPD-242B PAGE 3

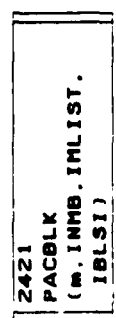
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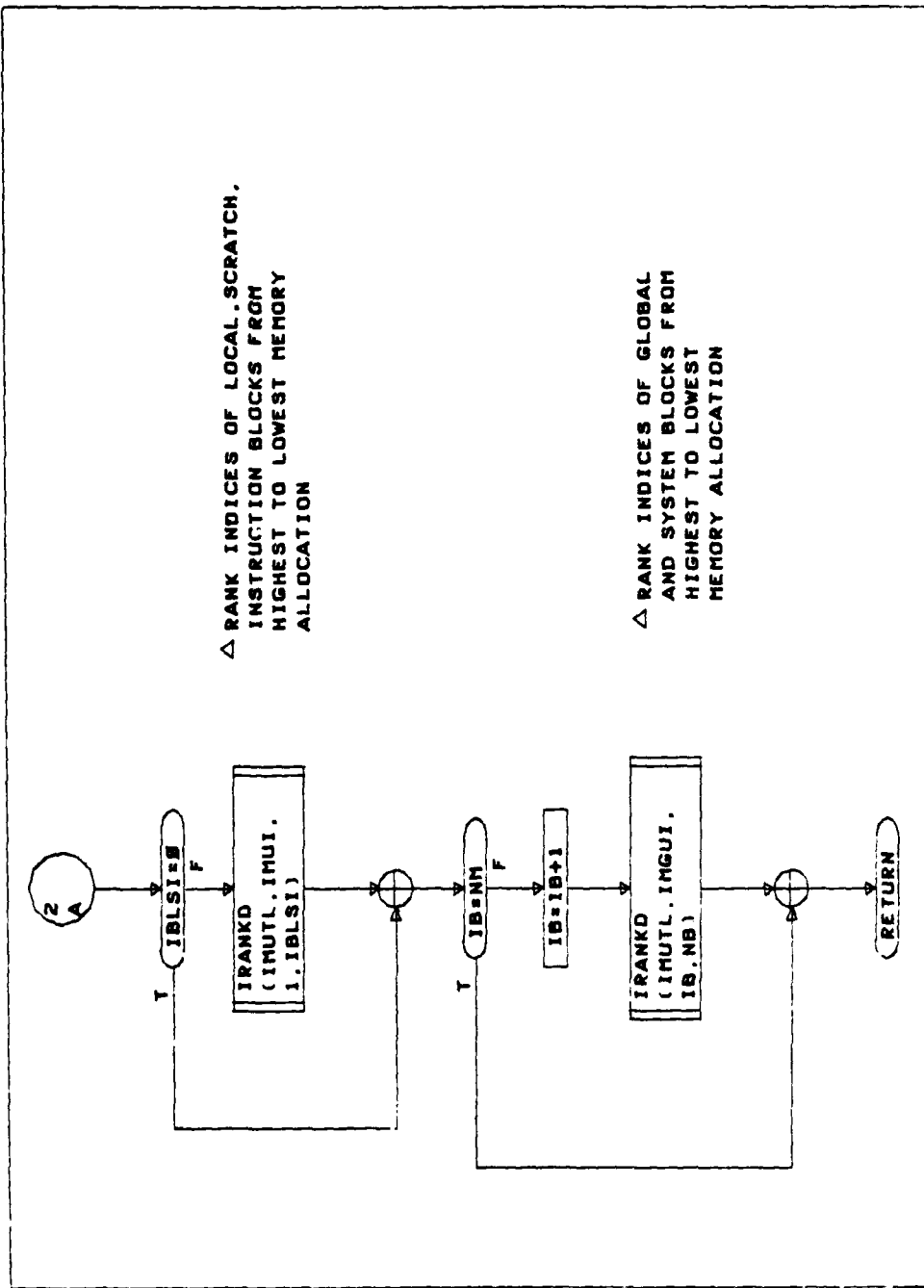
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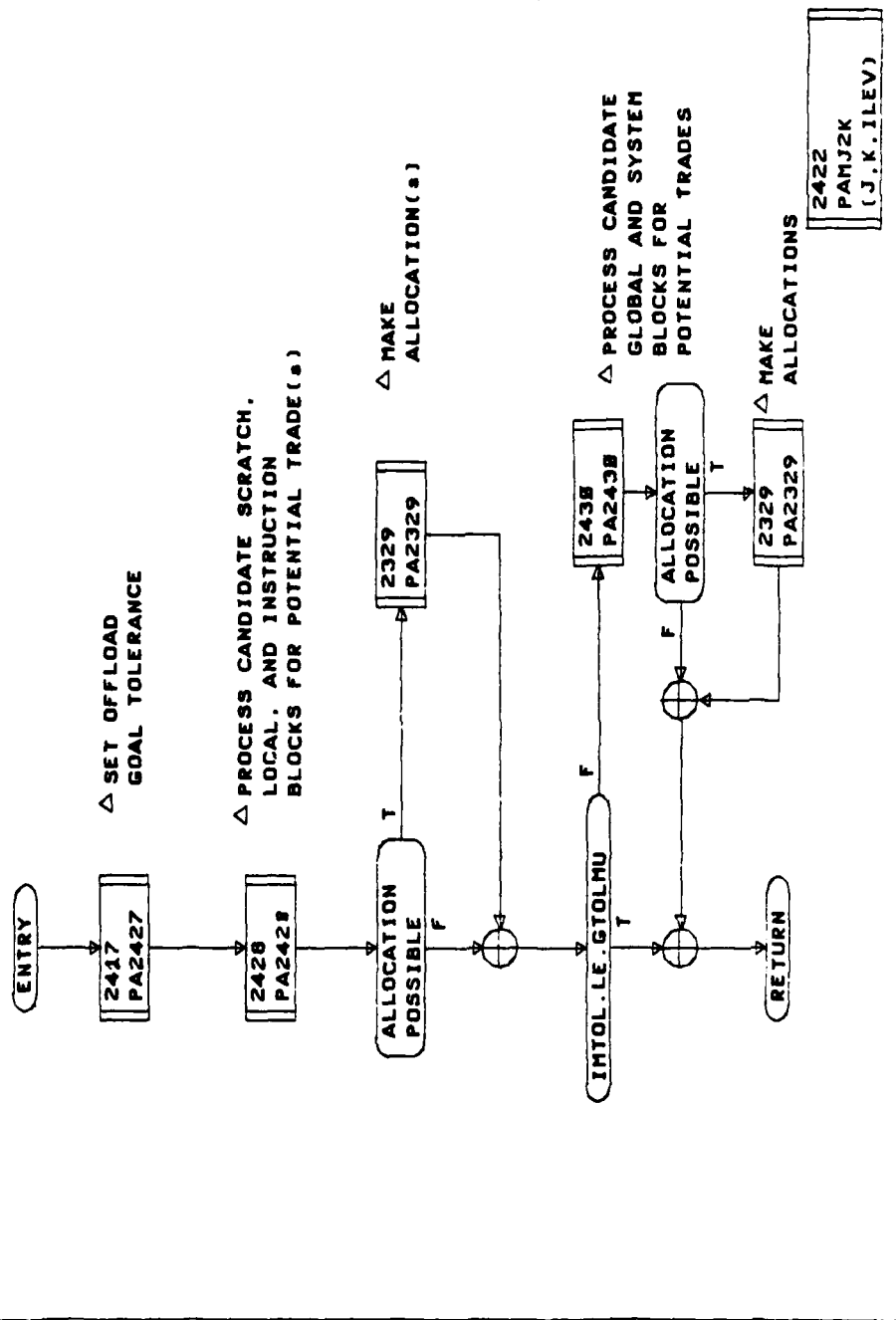


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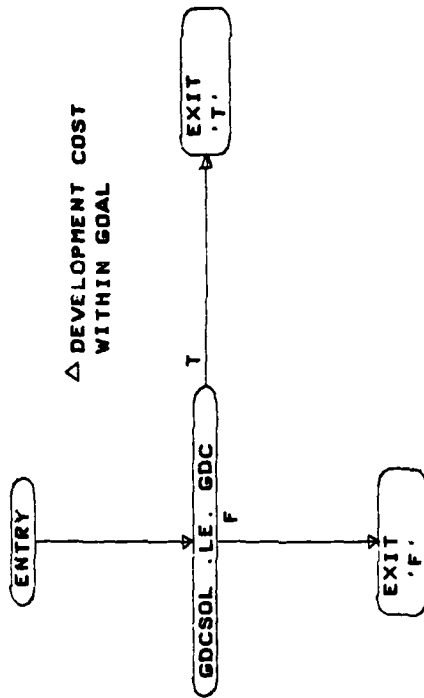


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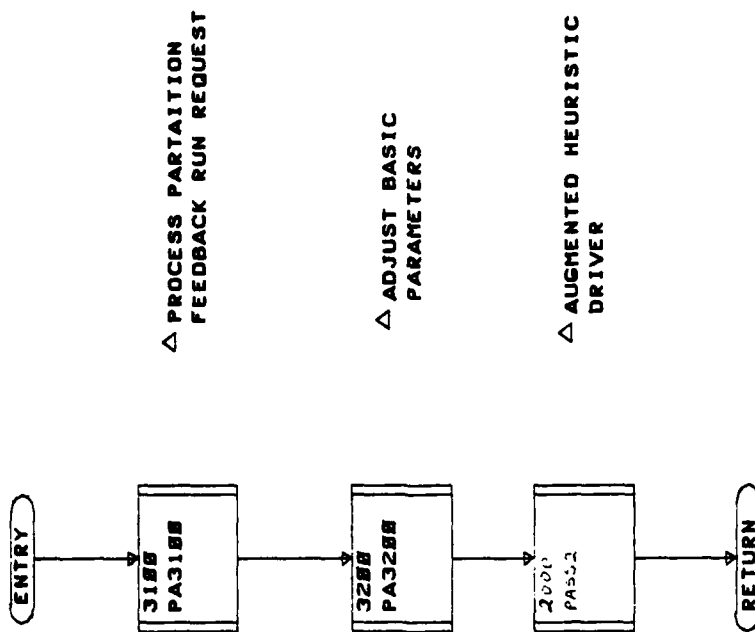
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251B
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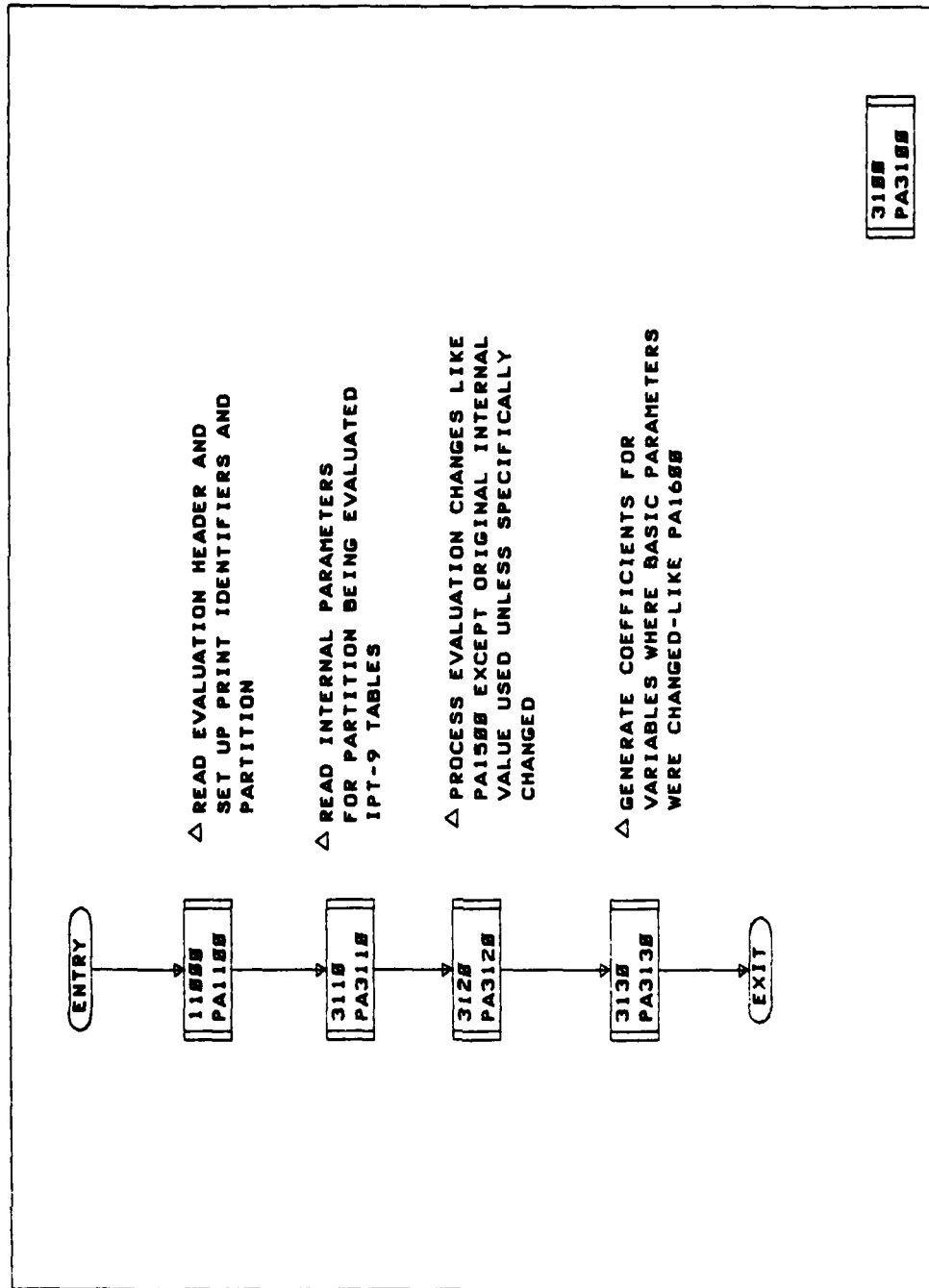
I 51E DATE 19-NOV-79 IO DEALS SEC PPO-251B PAGE 1

DEALS

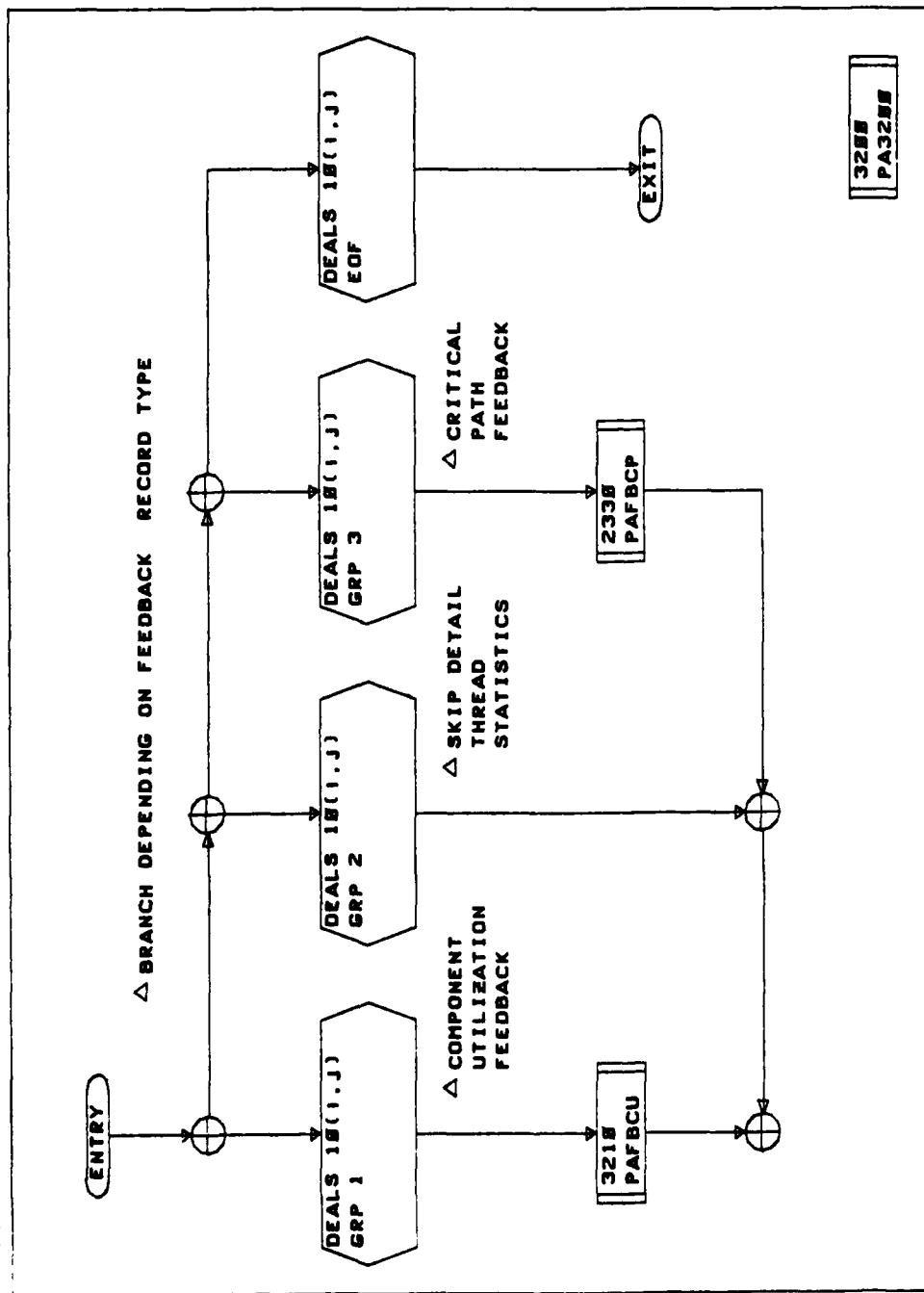


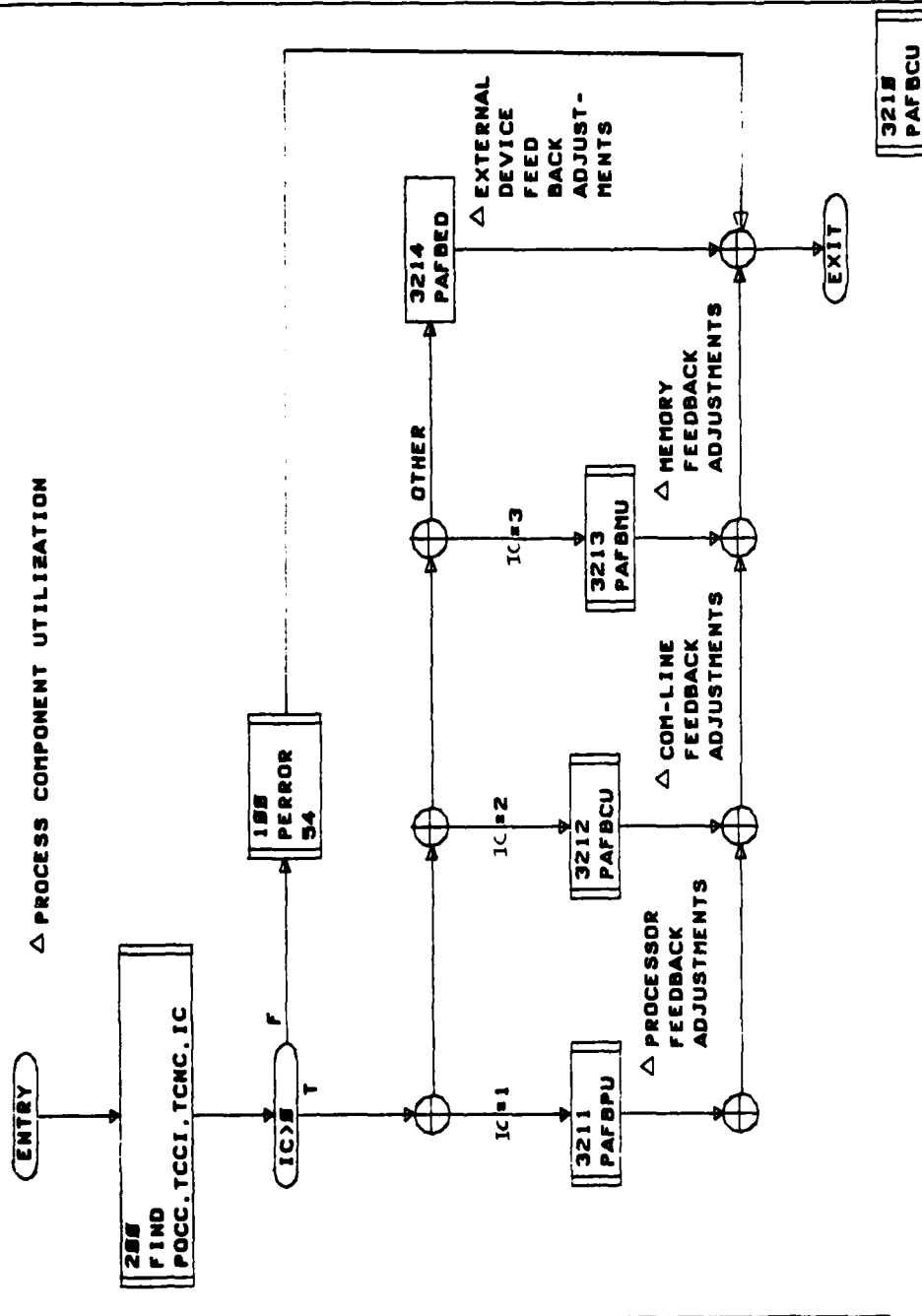
3888
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DEALS

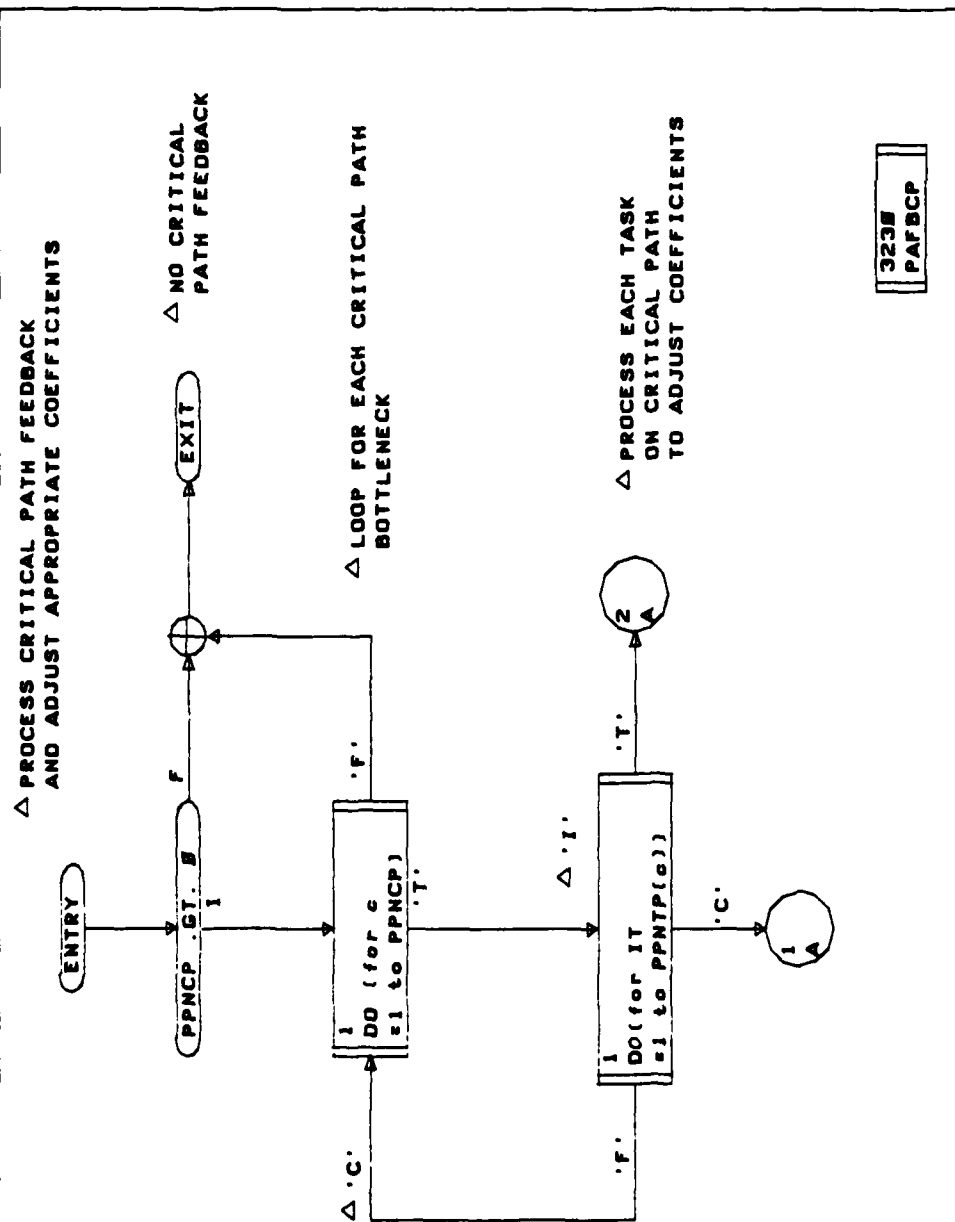


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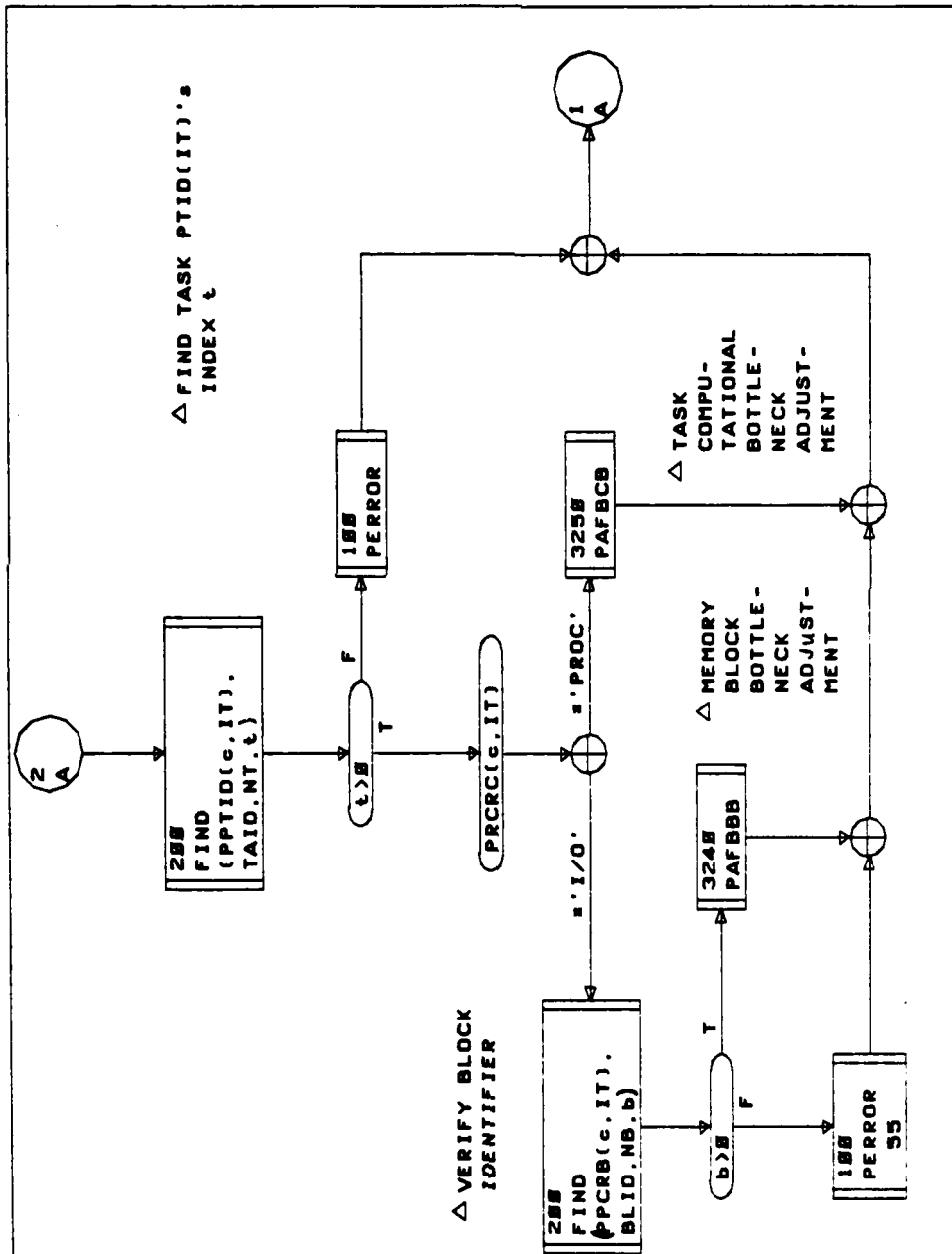




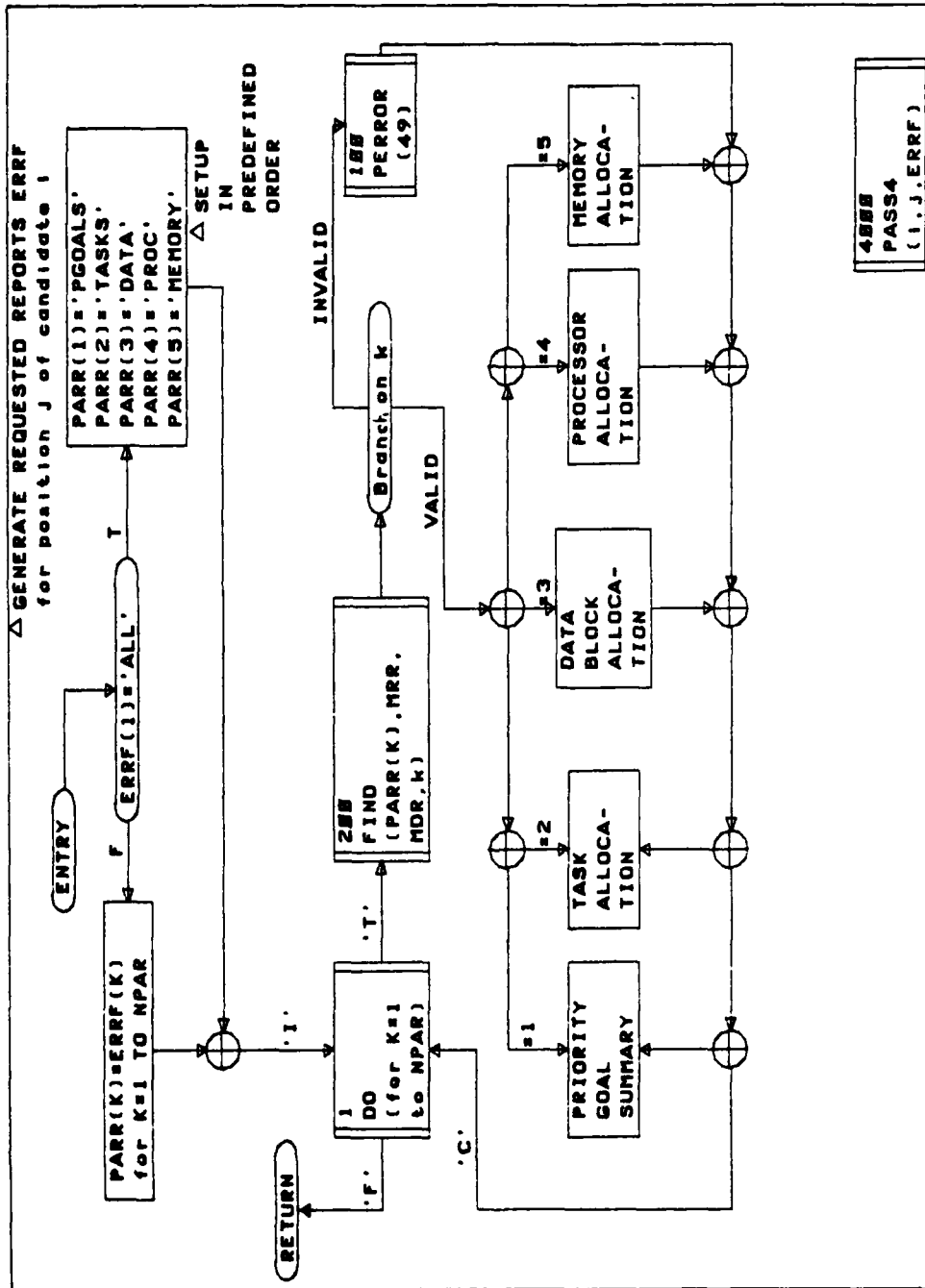
DIALS



DEALS



DEALS



ISSUE DATE 28-NOV-79 IO DEALS SEC PPD-40/NT PAGE 1

D.4 ERROR MESSAGES

MASTER ERROR CODES

ERROR	PPD	BRIEF DEFINITION
1	1100	Invalid technology data base identifier
2	1200	Invalid required interface file identifier
3	1210	Invalid technology type
4	1210	Invalid technology device
5	1211	Duplicate system or candidate processor device identifier
6	1211	Maximum processors exceeded
7	1213	Duplicate system or candidate memory device identifier
8	1212	Duplicate system or candidate device identifier
9	1212	Maximum communication devices exceeded
10	1213	Maximum memory devices exceeded
11	1300	Invalid baseline application file identifier
12	1310	Duplicate system block identifier
13	1310	Maximum blocks exceeded
14	1320	Maximum task identifier
15	1320	Maximum tasks exceeded
16	1400	Invalid candidate file identifier
17	1510	Undefined goal priority index
18	1510	Two goal priorities at same level
19	1510	Processor utilization goal is greater than absolute limit

MASTER ERROR CODES (CON'T)

ERROR	PPD	BRIEF DEFINITION
20	1510	Memory utilization goal is greater than absolute limit
21	1510	Development cost goal is greater than absolute limit
22	1510	Invalid default coefficient code
23	1520	Invalid goal index
24	1521	Invalid processor identifier
25	1521	User supplied processor goal greater than user supplied absolute limit
26	1521	Invalid processor coefficient level code
27	1522	Invalid memory identifier
28	1522	User specified memory goal greater than user specified absolute memory
29	1522	Invalid memory coefficient level code
30	1523	Invalid task identifier
31	1523	User supplied task cost goal is greater than user supplied absolute limit
32	1523	Invalid task coefficient level code
33	1540	Invalid constraint type
34	1541	Invalid task or processor identifier in constraint definition
35	1541	Duplicate task to processor constraint encountered
36	1541	Invalid task to processor constraint
37	1542	Invalid block or memory identifier in constraint definition

MASTER ERROR CODES (CON'T)

ERROR	PPD	BRIEF DEFINITION
38	1542	Duplicate block to memory constraint encountered
39	1542	Invalid block to memory constraint
40	2200	Saturated processor bottleneck detected
41	2200	Saturated memory bottleneck detected
42*	2300	Invalid goal index
43	2320	Fixed allocation has overloaded processor j
44	2320	Unable to offload processor j to be within absolute limit level
45	2320	Maximum processor balance iterations encountered
46	2320	Offloading has converged to single processor
47	2320	Least loaded processor unable to take on additional tasks
48*	2322	Invalid processor reallocate code
49	4000	Invalid report request
50	2420	Fixed allocation has overallocated memory j
51	2420	Unable to offload memory j to absolute limit level
52	2420	Maximum memory iterations
53	2420	Least loaded memory j unable to take additional blocks

*Fatal Algorithm Error

D.5 INTERNAL PARAMETERS

DEALS					ISSUE	DATE	19-DEC-79	ID	DEALS	SEC	IPT-9	PAGE	1
GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE	MEANING								
1	LIMITS, CONSTANTS, AND CODES												
	Maximum blocks	MB	Integers=488										
	Maximum columns of current optimization matrix	MC	Integers=18888										
	Maximum external devices	MED	Integers=28										
	Maximum replicates of any block	MH	Integers=4										
	Maximum number of distinct input and/or output blocks per task	MIO	Integers=6										
	Maximum memories	MM	Integers=28										
	Maximum processors	MP	Integers=28										
	Maximum partitions saved	MPS	Integers=3										
	Maximum communication devices	MQ	Integers=188										
	Maximum rows of current optimization matrix	MR	Integers=18888										

AD-A096 456 TELEDYNE BROWN ENGINEERING HUNTSVILLE ALA SYSTEMS DIV F/G 9/2
SOFTWARE PARTITIONING SCHEMES FOR ADVANCED SIMULATION COMPUTER --ETC(U)
FEB 81 S J CLYMER F33615-78-C-0013

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DEALS

GRP	PARAMETER NAME	MEMONIC	VALUES	UNITS/VALUE MEANING
	Maximum tasks	MT	Integer=155	
	Preemptive priority code 1:1 to 3	MPC (1)	2 characters	
		MPC (1)	'PB'	Processor utilization balance
		MPC (2)	'MB'	Memory utilization balance
		MPC (3)	'TC'	Task development cost
	Coefficient selection level codes 1:1 to 3	MCL (1)	1 character	
		MCL (1)	'A'	Average
		MCL (2)	'W'	Worst case
		MCL (3)	' '	Use default
	Master Restriction Codes	MRC (1)	1 character	
		MRC (1)	'F'	Fixed allocation
		MRC (2)	'I'	Initial allocation
		MRC (3)	'P'	Prohibited allocation

ISSUE

DATE 19-DEC-79

ID DEALS

SEC IPT-9

PAGE

2

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
2	CURRENT PROBLEM SIZING CONTROLS			
	Number of blocks	NB	Positive Integer 1.LE.NB.LE.MB	
	Number of columns in current optimizer matrix	NC	Positive Integer .LE.MC	
	Number of external devices	NED	Positive Integer .LE.MED	
	Number of memory devices	NM	Positive Integer .LE.MM	
	Number of processor devices	NP	Positive Integer .LE.MP	
	Number of communica- tion devices	NQ	Positive Integer .LE.MQ	
	Number of rows in current optimizer matrix	NR	Positive Integer .LE.MR	
	Number of tasks	NT	Positive Integer .LE.MT	
	Number of variables	NV	Positive Integer of .LE.(MC-2NR)	

ISSUE

DATE 15-NOV-70

ID

TOTALS

SEC IPT-9

PAGE

3

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
3	PRIORITY CONTROLS			
	Number of goals	NG	Integer	
			1.LE.NG.LE.3	
	Priority selected as goal L	GOAL (L)	Integer Code	
	L=1 to NG		=1	Processor Utilization Load Balance Heuristic
			=2	Memory Utilization Allocation Balance Heuristic
			=3	Minimize Development Cost Heuristic
	Priority default coefficient selection level	GDCS(L)	Integer Code =1 =2	Average Worst Case
	-Processor Coefficients	GDCS (1)		
	-Memory Coefficients	GDCS (2)		
	-Task Coefficients	GDCS (3)		

ISSUE DATE 21-NOV-79 ID DEALS SEC IPT-9 PAGE 4

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE	MEANING
	Processor utilization goal	GPU	real		
	Processor utilization limit	GPUU	real		
	Processor utilization tolerance	GTOLPU	real	=GPUU-GPU	
	Processor utilization solution measure	GPUSOL	real		
	Maximum processor balance iterations	MPITER	integer		
	Processor utilization penalty	GPNLT	real		
	Memory utilization goal	GMU	real		
	Memory utilization upper limit	GMUU	real		
	Memory utilization tolerance	GTOLMU	real	=GMUU-GMU	
	Memory utilization solution	GMUSOL	real		
	Maximum memory balance iterations	MMITER	integer		

ISSUE

DATE 21-NOV-79

ID DEALS

SEC IPT-9

PAGE

5

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Memory utilization penalty	GMPNLT	real	
	Development cost goal	GDC	real	
	Development cost upper limit	GDCU	real	
	Development cost tolerance	GTOLDC	real	=GDCU-GDC
	Development cost solution	GDCSOL	real	
	Maximum Development Cost Iterations	MCITER	integer	
	Number of processors for which the utilization is greater than supplied goal	NPGTG	non-negative integer 0.LE.NPGTG .LE. NP	
	Number of processors for which the utilization is greater than the upper limit	NPGTL	non negative integer 0.LE.NPGTL .LE.NPGTG	
	Number of memories for which the allocation is greater than supplied goal	NMG TG	non-negative integer 0.LE.NMG TG .LE.NM	

ISSUE DATE 21-NOV-79 ID DEALS SEC IPT-9 PAGE 6

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Number of memories for which the allo- cation is greater than supplied upper limit	NMGTL	non-negative integer 0.LE.NMGTL .LE. NMGTG	

ISSUE

DATE 21-NOV-79

10 DEALS

SEC IPT-9

PAGE

7

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
4	CURRENT PROCESSOR LIST			
	Number of distinct processor devices	CDPNT		
	For each distinct processor device d			
	Benchmark instruction flag i	CDPIF (d,i)	=8	Currently not in active solution
			=1	Currently in active solution

ISSUE DATE 28-DEC-79 IO DEALS SEC IPT-9 PAGE 8

DEALS

GRP	PARAMETER NAME	MEMORIC	VALUES	UNITS/VALUE MEANING
	Per processor psl to NP			
	-Identifier	CDPID (p)	18 characters	
	-Technology device index	CDPTI (p)	Integer > 8	
	-Operating system	CDPOS (p)	18 char code	
	-Active task levels	CDPTL (p)	Integer > 8	
	-Language l=1 to 3	CDPL (p,L)	18 Char code	
	-Goal utilization	CDPGU (p)	real	
	-Maximum acceptable utilization	CDPMU (p)	real	
	-Current solution utilization	CDPCU (p)	real	
	-Current utilization deviation for goal	CDPCD (p)	real	
	-Coefficient selection level	CDPCD (p)	Integer code =1 =2	Average Worst Case
	-Current solution SW development cost	CDPDC (p)		

ISSUE

DATE 19-DEC-79

ID DEALS

SEC IPT-9

PAGE

9

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
5	CURRENT MEMORY LIST			
	For memory m=1 to NM			
	-Identifier	CDMID (m)	15 characters	
	-Technology device index	CDMTI (m)	Integer > 5	
	-Sizing			
	.Unit Index	CDMSU (m)	Integer	
	.Amount	CDMSA (m)	Integer > 5	
	.Total bits	CDMSZ (m)	real > 5	
	-Goal utilization	CDMGU (m)	real	
	-Maximum acceptable utilization	CDMMU (m)	real	
	-Current solution utilization	CDMCU (m)	real	
	-Current utilization deviation from goal	CDMCD (m)	real	
	-Coefficient selection level	CDMCL (m)	integer code s1 s2	Average Worst Case
	-Current solution total memory access time	CDMTA (m)		

ISSUE

DATE 19-DEC-79

ID DEALS

SEC IPT-9

PAGE

15

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
6	CURRENT COMMUNICATION LINK LIST			
	For communication device q1 to NQ			
	-Identifier	CDQID (q)	18 characters	
	-Technology device index	CDQTI (q)	positive integer	
	-Number of inter- facing devices	CDQND (q)	positive integer	
	-Interfacing device 1 = 1 to CDQNI (q)			
	.Type	CDLIT(q,1)	Integer Code =1 =2 =3 =4,5,...,14	for processor illegal for current algorithms memory for external devices
	.Candidate Index	CDLII(q,1)	Integer > 8	
	.Priority Level	CDLIP(q,1)	Integer > 8	

ISSUE DATE 19-DEC-79 ID DEALS SEC IPT-9 PAGE 11

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
7	CURRENT EXTERNAL DEVICE LIST For device ds1 to NED -Identifier -Type Index -Technology device Index -Number of system data blocks -For each data block ds1 to CDEDB(d) .Block Index	 CDEID (d) CDETY (d) CDETI (d) CDENB (d) CDEBI(d,b)		

ISSUE DATE 19-DEC-79 ID DEALS SEC IPT-9 PAGE 12

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
0	TASK/PROCESSOR ALLO- CATION AND RESTRIC- TIONS			
	Task t processor p map	TPMAP (t.p.1)		
		TPMAP (t.p.1)	0,1,....,Nt	current task t ex- ecutions allocated to processor p
		TPMAP (t.p.2)	0,1,....,Nt	lower bound on task t executions on processor p
		TPMAP (t.p.3)	0,1,....,Nt	upper bound on task t executions on processor p
		TPMAP (t.p.4)	Integer Code	
			=0	No user allocation input (default value)
			=1	User allocation processed

ISSUE DATE 19-DEC-79 ID DEALS SEC IPT-9 PAGE 13

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	Task t processor p coefficient values			
	Time for task t execution on pro- cessor p	TPVAL (t.p.1)	real > 0	milliseconds
	Resource task management coeffi- cient for task t on processor p if time or data enabled	TPVAL (t.p.2)	real > 0	microseconds
	Resource task management per task t execution on pro- cessor p for slaved enabled task	TPVAL (t.p.3)	real > 0	microseconds
	The cost coeffi- cient for developing	TPVAL (t.p.4)	real > 0	manyears
	The cost coeffi- cient for resource management of task t development on processor p	TPVAL (t.p.5)	real > 0	manyears

DEALS

GRP	PARAMETER NAME	MPHONIC	VALUES	UNITS/VALUE MEANING
9	MEMORY/PROCESSOR COMMUNICATION ALLO- CATIONS, RESTRICTIONS			
	Basic communication between memory m and processor p			
	-Read access	MPMAP (m.p.1)	Real .LE. B otherwise	no access read rate bits/ second
	-Write access	MPMAP (m.p.2)	Real .LE. B otherwise	no write access write rate bits/ second
	-Number of current solution entries	MPMAP (m.p.3)	Non-negative integer	

ISSUE DATE 21-NOV-79 ID DEALS SEC IPT-9 PAGE 15

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	For each current solution entry e	MPSOL		
	.Task index t	MPSOL (m.p.e.1)		
	.Block index b	MPSOL (m.p.e.2)		
	.Type of access	MPSOL (m.p.e.3)	Integer code =1 read only =2 write only =3 read and write	
	.Number of task executions on p making access to memory m	MPSOL (m.p.3.4)	Integer	
			.GE. 1	Must be at least one for entry
			.LE. NT Where ts MPSOL(m.p.e.1)	At most all task t executions are on processor p and utilize block b from memory m

ISSUE

DATE 19-DEC-79

ID DEALS

SEC IPT-9

PAGE

16

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
1B	MEMORY/BLOCK ALLOCATION RESTRICTIONS. AND COEFFICIENTS			
	Memory m block b map			
		MBMAP (m.b.1)	S.1	current allocations
		MBMAP (m.b.1)		0-not allocated 1-allocated
		MBMAP (m.b.2)	S.1	lower bound for 0-does not have to be allocated 1-must be allocated
		MBMAP (m.b.3)	S.1	upper bound for 0-cannot be allocated 1-may be allocated
		MBMAP (m.b.4)	S.1	user option processed 0-not processed (default) 1-processed
		MBVAL(m.b)	real	length of block b if stored on memory m

ISSUE DATE 21-NOV-79 ID DEALS SEC IPT-9 PAGE 17

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
11	MASTER BLOCK LIST For each block b=1 to NB			
	- Identifier	BLID (b)		
	- Level	BLLEV (b)	Integer code =1 =2 =3 =4 =5	System level block Global block Local block Scratch block Instruction block
	- Discipline	BLOSP (b)	Integer code	Must match technology data base block discipline codes in IOPT-5
	- Number of suitable memories	BLNSM (b)	Integer .GE. 8	
	- Suitable Memory List 1=1 to BLNSM(b)	BLSMH (b,1)	Positive integers	Indices to candidate memory devices
	- Maximum Records	BLMXR (b)	Positive integers	

ISSUE	DATE	21-NOV-79	ID	DEALS	SEC	IPT-9	PAGE	18
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DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	-Record length			
	.Bits/Byte	BLRBI (b)	positive integer	bits
	.Bytes/word	BLRBY (b)	positive integer	bytes
	.Minimum Words	BLRW(b,1)	positive integer	words
	.Average Words	BLRW(b,2)	positive integer	words
	.Maximum Words	BLRW(b,3)	positive integer	words
	-Number of tasks referencing block b	BLNTR (b)		
	-List of tasks referencing block b for a1 to BLNTR(b)			
	.Task index	BLTID (b,e)		
	.Reference index	BLTRF (b,e)	a1 a2 a3	as input as output as update

ISSUE DATE 19-DEC-79 ID DEALS SEC IPT-9 P: 19

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
12	MASTER TASK LIST For each task t=1 to NT			
	- Identifier	TAID (t)	6 characters	
	- Source code index	TASC (t)	positive integer	
	- Number of benchmark instruction references in task instruction mix list	TANIM(t)	Positive Integer .GE. 1	
	- Instruction mix list for each benchmark reference i=1 to TANIM(t)	TAIMX (t,i,j)		
	- Benchmark instruction index	TAIMX (t,i,1)		
	- Count for sizing Average	TAIMX (t,i,2)	Positive Integer	
	- Worst Case	TAIMX (t,i,3)	Positive Integer	

DATE 19-DEC-79 ID DEALS SEC IPT-9 PAGE 28

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	.Execution counts for timing			
	Average	TAIMX (t,1,4)	Positive integer	
	Worst Case	TAIMX (t,1,5)	Positive integer	
	-Overlay flag	TAOLF (t)	#B #1	not an overlay overlay
	-Number of task I/O blocks	TANIO (t)	positive integer	
	-for each block i=1 to TAOIO(t)			
	.Block index	TAIOB(t,i)	positive integer	
	.How referenced index	TAHBR(t,i)	positive integer #1 #2 #3	Input Output Update

ISSUE DATE 28-DEC-79 ID DEALS SEC IPT-9 PAGE 21

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	.When referenced index	TANBR(t,i)	positive integer	
			=1	START
			=2	ALONG
			=3	END
	.Records read per task t execu- tion	TARR (t,i,k)	positive integer	k=1 minimum k=2 average k=3 maximum
	.Fraction of records read from block i task t based upon current coefficient sel- ection level	TARRF (t,i)	Positive real FIG.5	
	.Records output per task t execu- tion	TARW (t,i,k)	Positive Integer	k=1 minimum k=2 average k=3 maximum
	.Fraction of records written to block i by task t based upon current coefficient sel- ection level	TARWF (t,i)	positive real FIG.5	

ISSUE DATE 28-DEC-79 ID DEALS SEC IPT-9 PAGE 22

DEALS

SRP	PARAMETER NAME	HMEMONIC	VALUES	UNITS/VALUE MEANING
	-Task enablement index	TAEN (t)	positive integer code s1 s2 s3	
	-Master Task	TAMT (t)	6 characters	
	-Maximum execute time	TAMET (t)	real	
	-Frequency	TAFRO (t)	real	iterations per second

ISSUE

DATE 19-DEC-79

ID DEALS

SEC IPT-9

PAGE

23

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
	-Task development cost			
	.Goobj	TADCG (t)	real	manyyears
	.Upper limit	TADCU (t)	real	manyyears
	.Current solution	TADCS (t)	real	manyyears
	.Current deviation from goal	TADCD (t)	real	manyyears
	.Current task cost index	TADCI (t)	integer	
	.Number of processor currently allocated to task t	TADCP (t)	integer .GE. 1	
	.List of processors for est to TADCP (t)	TADCL(t,e)	integer	candidate processor index
	-Coefficient generation level	TACLS (t)	integer code =1 =2	Average Worst Case

15.7E

DATE 28-DEC-79

ID DEALS

SEC IPT-9

PAGE

24

DEALS

GRP	PARAMETER NAME	MNEMONIC	VALUES	UNITS/VALUE MEANING
13	BASELINE STATIC LOAD			
	Evaluation interval	BLPER	Positive Real	Seconds
	Number of threads active	BLPAT	Non-negative Integer	
	For each active thread k			
	.Number of tasks [BLPAT]	BLTNT(k)	Positive Integer .LE.NT	
	.Task Indices [BLPAT,BLTNT]	BLTIN(k,g)	Positive Integer .LE.NT	
	Number of distinct parallel task groups	BLPAG	Non-negative Integer	
	For each active parallel group g			
	.Number of tasks [BLPAP]	BLGNT(g)	Positive Integer .LE. NT	
	.Task Indices [BLPAP,BLGNT]	BLGIN(g,i)	Positive Integer .LE. NT	

ISSUE DATE 28-DEC-79 ID DEALS SEC IPT-9 PAGE 25

DATE
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-8